Version	2.2
Total pages	16
Date	2005.07.11

Product Specification

10.4″ SVGA Color TFT-LCD Module

MODEL NAME: A104SN01 V0

(.◆.) Preliminary Specification
( ) Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
1	20/Feb/2004	-	First Draft
2	06/Apr/2005		Interface change to LVDS
3	30/June/2005		Reliability test items modification (Vibration & Mechanical Shock)

Contents:

Appendix:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	800RGB(H)×600(V)	
2	Active area (mm)	211.2(H) x 158.4(V)	
3	Screen diagonal (inch)	10.4”	
4	Pixel pitch (mm)	0.264(H)×0.264(V)	
5	Color configuration	R. G. B. stripe	
6	Overall dimension (mm)	243.0x184.0x24.0	Note 1
7	Weight (g)	680	

Note 1: Refer to Fig. 1 (P.12)

B. Electrical specifications

1. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power Voltage	V_{DD}	Ta= 25℃	-0.3	3.4	V	
	VBL		10.8	13.2	V	NOTE1
	DIMMER		0	5	V	
	REV		0	3.4	V	
Operating Temperature	To	-	-10	60	℃	Ambient Temperature
Storage Temperature	Ts	-	-20	70	℃	Ambient Temperature

NOTE1: VBL is for inverter power, and typical is 12V.

2. Electrical characteristics

2.1 Typical operating conditions

Item		Symbol	Min.	Type	Max.	Unit	Remark
Power support		VDD	3.15	3.3	3.4	V	
		VBL	10.8	12	13.2	V	
		VDIMMER	5	-	0		NOTE1
VCDC			2.3	3.3	4.6	V	NOTE2
Input signal voltage	H level	VIH	2.0		VDD	V	
	L level	VIL	0		0.8	V	

NOTE1: When VDIMMER =0V,is the most brightness, and VDIMMER=5V brightness become weak.

NOTE2:

2.2 Current consumption

Item	Symbol	Condition	Min.	Type	Max.	Unit
Current for PCB	IVDD	VDD=3.3V	-	660	770	mA
Current for Inverter	IVBL	VBL=12V Vcon=0V	-	600	720	mA

2.3 Inrush Current and Inrush time

Item	Symbol	Condition	Min.	Type	Max.	Unit
Inrush Current for PCB	Ivdsh	VDD=3.3V	-	1.0	1.2	A
	Tlvdsh			15	10	ms
Inrush Current for Inverter	Ivbsh	VBL=12V Vcon=0V	-	13.7	15.07	A
	Tlvbsh			30	33	us

3 Signal Description

3.1 Connector

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Digital Signal Connector
Manufacturer	Kyocera Elco
Type / Part Number	04 6274 042 000 800

3.2 Pin assignment

Pin No.	Signal Name	Pin No.	Signal Name
1	DGND	2	RxIN0＋
3	RxIN0-	4	DGND
5	RxIN1＋	6	RxIN1-
7	DGND	8	RxIN2＋
9	RxIN2-	10	DGND
11	CKIN＋	12	CKIN-
13	DGND	14	REVERSE
15	DGND	16	DIMMER
17	DGND	18	DGND
19	DGND	20	DGND
21	DGND	22	DGND
23	DGND	24	DGND
25	VDD	26	VDD
27	VDD	28	VDD
29	VDD	30	VDD
31	VDD	32	VDD
33	VBL_GND	34	VBL_GND
35	VBL_GND	36	VBL_GND
37	VBL_GND	38	VBL
39	VBL	40	VBL
41	VBL	42	VBL

3.3 Signal Description

Signal Name	Description
RxIN0-, RxIN0+	**LVDS differential data input(Red0-Red5, Green0)**
RxIN1-, RxIN1+	**LVDS differential data input(Green1-Green5, Blue0-Blue1)**
RxIN2-, RxIN2+	**LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DE)**
RxCLKIN-, RxCLKIN0+	**LVDS differential clock input**
VDD	**+3.3V Power Supply**
DGND	**Ground of PCB**
VBL_GND	**Ground of Inverter**
VBL	**+12V Power Supply for inverter**
REVERSE	**Reverse function for Panel display**
DIMMER	**To control brightness of backlight**

Internal circuit of LVDS inputs are as following.

Signal Name	Description	
+RED5 **+RED4** **+RED3** **+RED2** **+RED1** **+RED0**	**Red Data 5 (MSB)** **Red Data 4** **Red Data 3** **Red Data 2** **Red Data 1** **Red Data 0 (LSB)** Red-pixel Data	**Red-pixel Data** **Each red pixel's brightness data consists of these 6 bits pixel data.**
+GREEN 5 **+GREEN 4** **+GREEN 3** **+GREEN 2** **+GREEN 1** **+GREEN 0**	**Green Data 5 (MSB)** **Green Data 4** **Green Data 3** **Green Data 2** **Green Data 1** **Green Data 0 (LSB)** Green-pixel Data	**Green-pixel Data** **Each green pixel's brightness data consists of these 6 bits pixel data.**
+BLUE 5 **+BLUE 4** **+BLUE 3** **+BLUE 2** **+BLUE 1** **+BLUE 0**	**Blue Data 5 (MSB)** **Blue Data 4** **Blue Data 3** **Blue Data 2** **Blue Data 1** **Blue Data 0 (LSB)** Blue-pixel Data	**Blue-pixel Data** **Each blue pixel's brightness data consists of these 6 bits pixel data.**
RxCLKIN-	Data Clock	**The typical frequency is 40 MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.**
DE	Data Enable	**This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.**
VSYNC	Vertical Sync	**The signal is synchronized to RxCLKIN-.**
HSYNC	Horizontal Sync	**The signal is synchronized to RxCLKIN- .**

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

3.4 Signal Electrical Characteristics

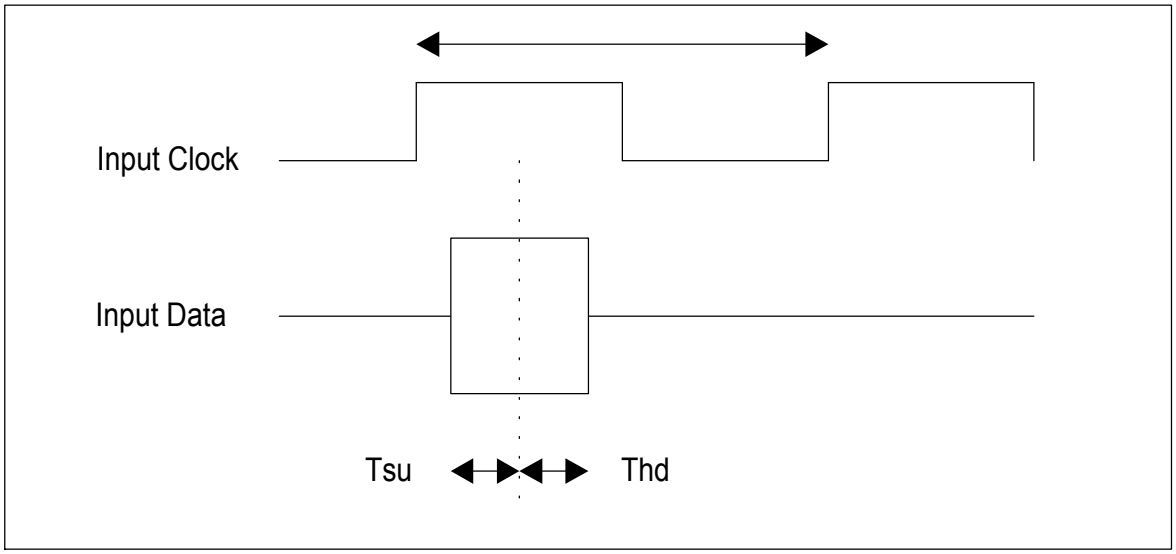
It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	**Differential Input High Voltage(Vcm=+1.2V)**		**100**	**[mV]**
Vtl	**Differential Input Low Voltage(Vcm=+1.2V)**	**-100**		**[mV]**

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (F)	20MHz	**85MHz**
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	



4. Timing Characteristics

Basically, interface timing should match the VESA 800x600 /60Hz(VG901101) manufacturing guide line timing.

4.1 SVGA MODE

(a) DE mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	**Fck**	**36**	**40**	**50**	**MHz**	
Horizontal blanking	**Thb1**	**18**	**256**	**624**	**Clk**	
Vertical blanking	**Tvb1**	**3**	**28**	**184**	**Th**	

(b) HV mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	**Fck**	**36**	**40**	**50**	**MHz**	
Hsync period	**Th**	**1018**	**1056**	**1424**	**Clk**	
Hsync pulse width	**Thw**	**2**	**128**	**-**	**Clk**	
Hsync front porch	**Thf**	**8**	**40**	**-**	**Clk**	
Hsync back porch	**Thb**	**4**	**88**	**-**	**Clk**	
Hsync Active		**-**	**800**	**-**	**Clk**	
Hsync blanking	**Thb1**	**218**	**256**	**624**	**Clk**	
Vsync period	**Tv**	**625**	**628**	**784**	**Th**	
Vsync pulse width	**Tvw**	**1**	**4**	**-**	**Th**	
Vsync front porch	**Tvf**	**0**	**1**	**-**	**Th**	
Vsync blanking	**Tvb1**	**25**	**28**	**184**	**Th**	
Vsync Active		**-**	**600**	**-**	**Th**	
Hsync/Vsync phase shift	**Tvpd**	**0**	**320**	**-**	**Clk**	

Item	Symbol	Value	Unit	Description
Horizontal display start	**The**	**216**	**Clk**	**After falling edge of Hsync, counting 216clk, then getting valid data from 217th clk's data.**
Vertical display start	**Tve**	**27**	**Th**	**After falling edge of Vsync, counting 27th, then getting 28th Th's data.**

b. VGA MODE

(a)DE mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	**Fck**	**-**	**25.2**	**36**	**MHz**	
Horizontal blanking	**Thb1**	-	**144**	**192**	**Clk**	
Vertical blanking	**Tvb1**	-	**29**	**29**	**Th**	

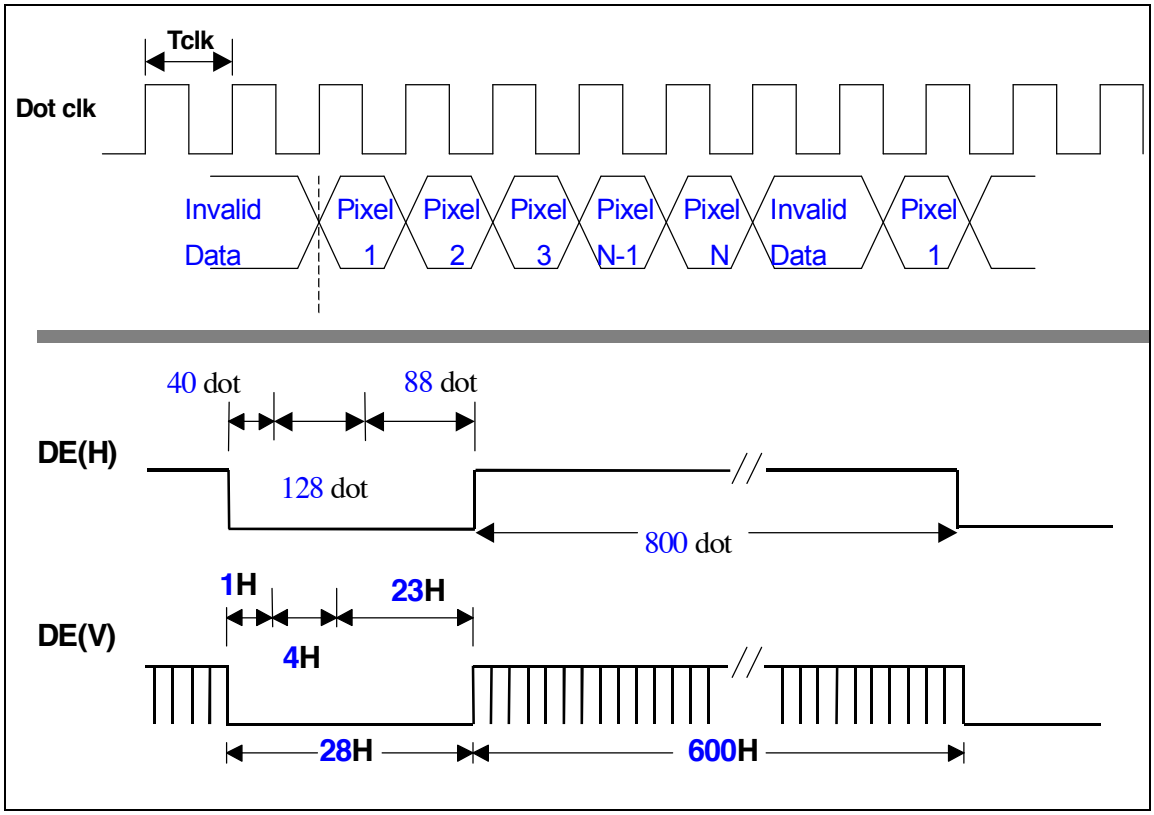
(b)HV mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	**Fck**	**-**	**25.2**	**36**	**MHz**	
Hsync period	**Th**	**680**	**800**	**832**	**Clk**	
Hsync pulse width	**Thw**	**-**	**96**	**120**	**Clk**	
Hsync front porch	**Thf**	**-**	**8**	**56**	**Clk**	
Hsync back porch	**Thb**	**-**	**40**	**80**	**Clk**	
Hsync blanking	**Thb1**	**-**	**144**	**192**	**Clk**	
Hsync Active		**-**	**640**	**-**	**Clk**	
Hsync left border		**-**	**8**	**-**	**Clk**	
Hsync right border		**-**	**8**	**-**	**Clk**	
Vsync period	**Tv**	**509**	**525**	**-**	**Th**	
Vsync pulse width	**Tvw**	**-**	**2**	**3**	**Th**	
Vsync front porch	**Tvf**	**-**	**2**	**-**	**Th**	
Vsync blanking	**Tvb1**	**-**	**29**	**-**	**Th**	
Vsync active		**-**	**480**	**-**	**Th**	
Hsync/Vsync phase shift	**Tvpd**	**0**	**320**	**-**	**Clk**	
Vsync top border		**-**	**8**	**-**	**Th**	
Vsync bottom border		**-**	**8**	**-**	**Th**	

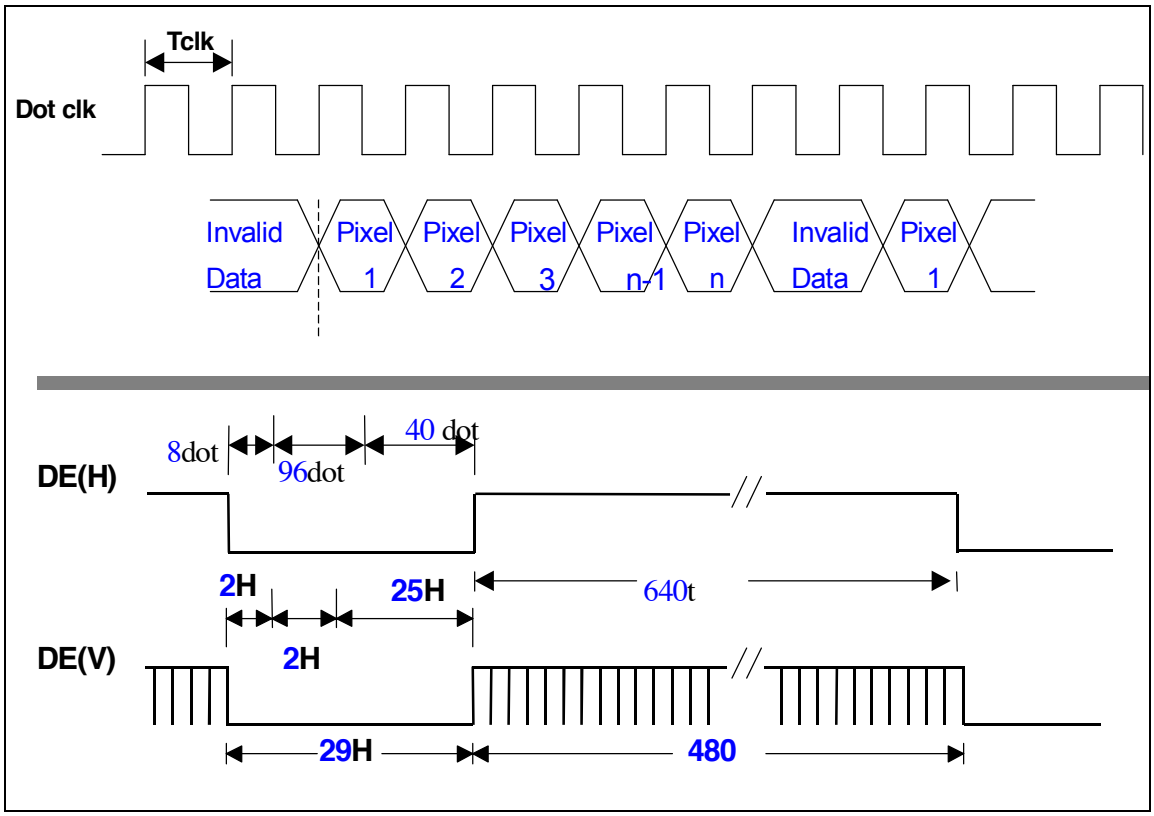
Item	Symbol	Value	Unit	Description
Horizontal display start	**The**	**144**	**Clk**	**After falling edge of Hsync, counting 144clk, then getting valid data from 145th clk's data.**
Vertical display start	**Tve**	**35**	**Th**	**After falling edge of Vsync, counting 35th, then getting 36th Th's data.**

5. Timing Definition

a. SVGA mode



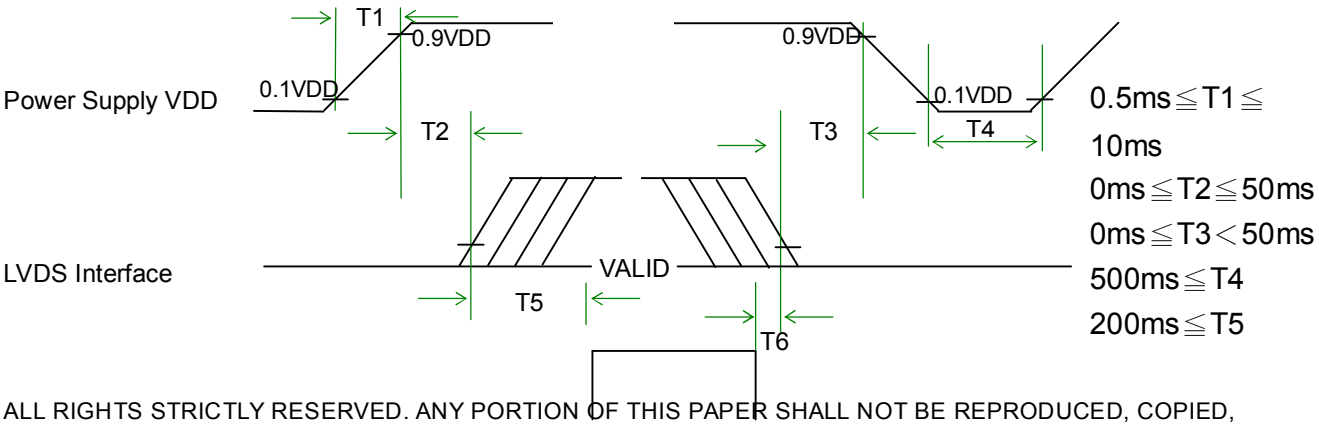
b. VGA Mode



6. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

Sequence of Power-on/off and signal-on/off



Backlight On

Apply the lamp voltage within the LCD operating range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal.

C. Optical specification (Note 1, Note 2, Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ =0°	- -	10 25	25 50	ms ms	Note 4,6
Contrast ratio		CR	At optimized Viewing angle	200	350	-	-	Note 5,6
Viewing angle	Upper Lower Left Right		CR≧10	30 50 50 50	40 60 60 60	- - - -	Degree	Note 6,7
Lamp Life Time		-	-	10,000	-	-	-	Note 8
Luminance		Y_L	θ =0°	400	450	-	cd/m^2	Note 9
White chromaticity		X	θ =0°	0.28	0.33	0.38	-	-
		Y	θ =0°	0.30	0.35	0.40	-	

Note 1 : Ambient temperature =25℃. And lamp current I_L = 5.2 mArms.

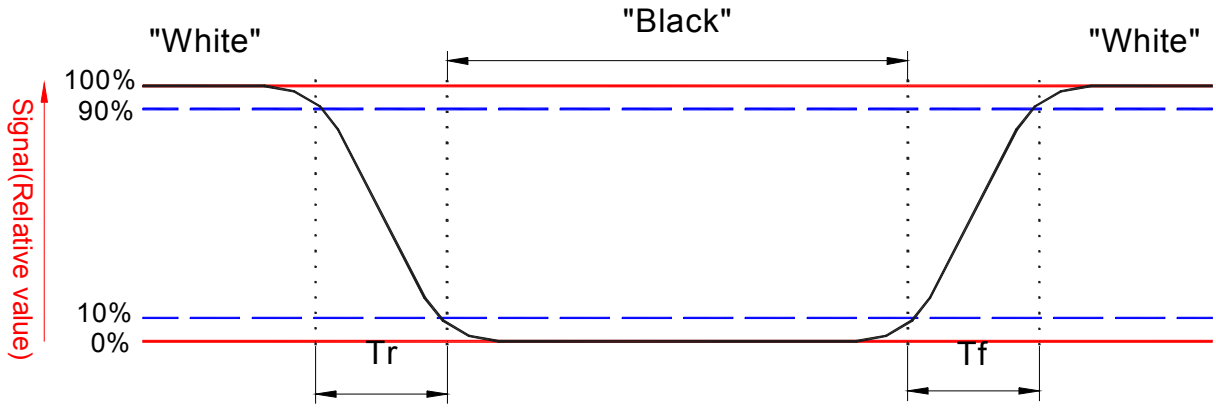
Note 2: To be measured in the dark room.

Note 3 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7, after 30 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Note 4. White $Vi=V_{i50} + 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

“±” means that the analog input signal swings in phase with V_{COM} signal.

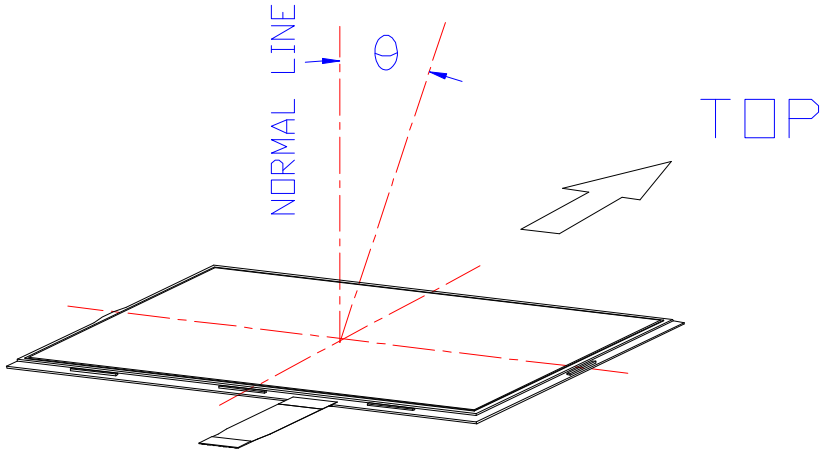
“$\overline{+}$” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

Refer to figure as below.



Note 8. The “Lamp life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C, I_L=5.2mA.

Note 9. Transmission is defined as follow:(θ =0°)

Transmission = B1/B2

B1=Photo detector output voltage when measuring the brightness of the LCD panel placed on the light source with no applied voltage

B2=Photo detector output voltage when measuring the light source

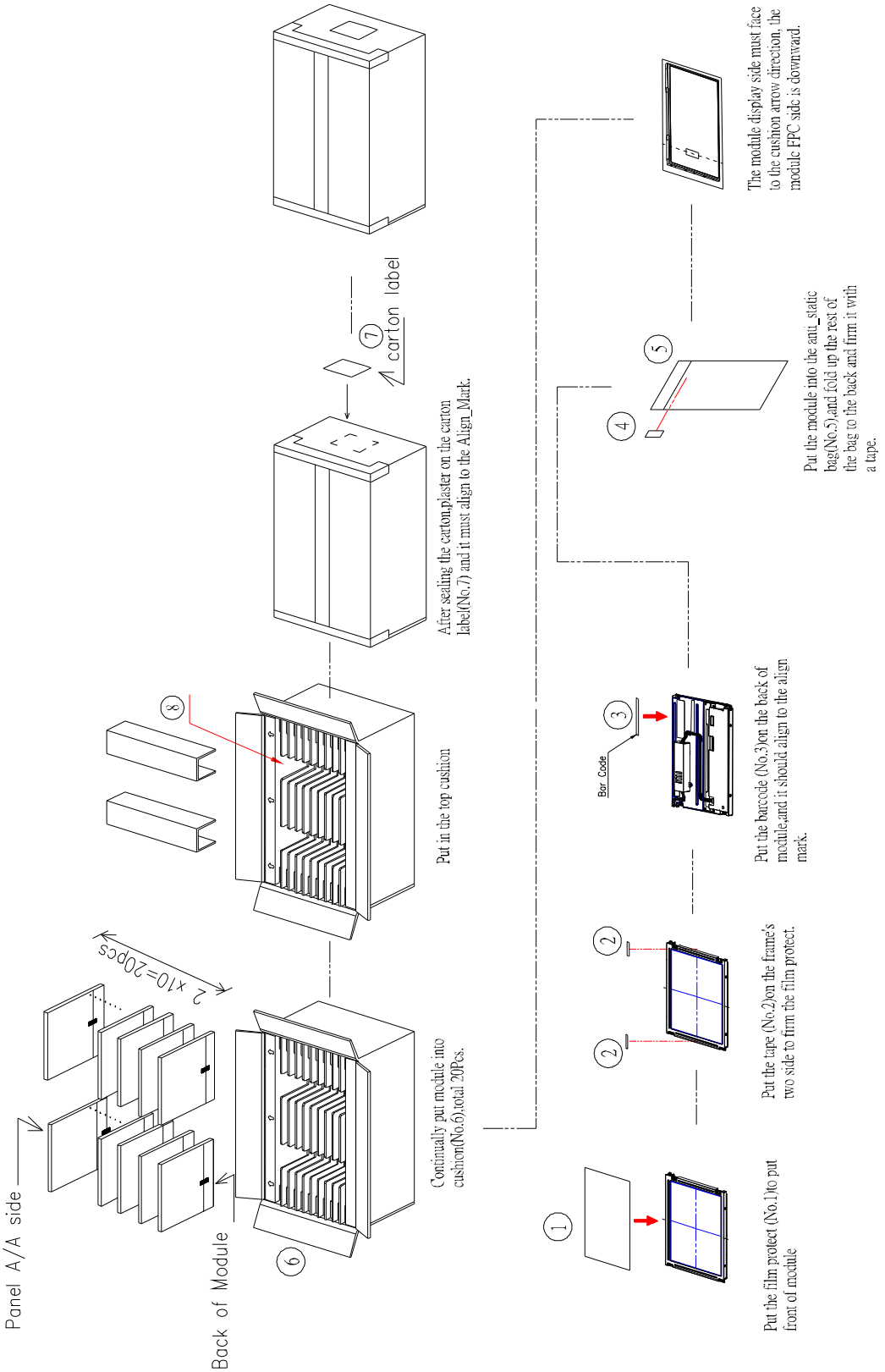
D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -20℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 50℃, 80% RH 240Hrs	Operation
6	Heat shock	-20℃~70℃/ 50 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	1.5G, 10Hz ~ 200Hz ~ 10Hz 30 minutes for each Axis (X, Y, Z)	Non-Operation
9	Mechanical shock	100G/6ms,±X,±Y,±Z once for each direction	Non-Operation
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient Temperature.

Note2: All the cosmetic and optical specifications are judged before the reliability stress.

E. Packing form



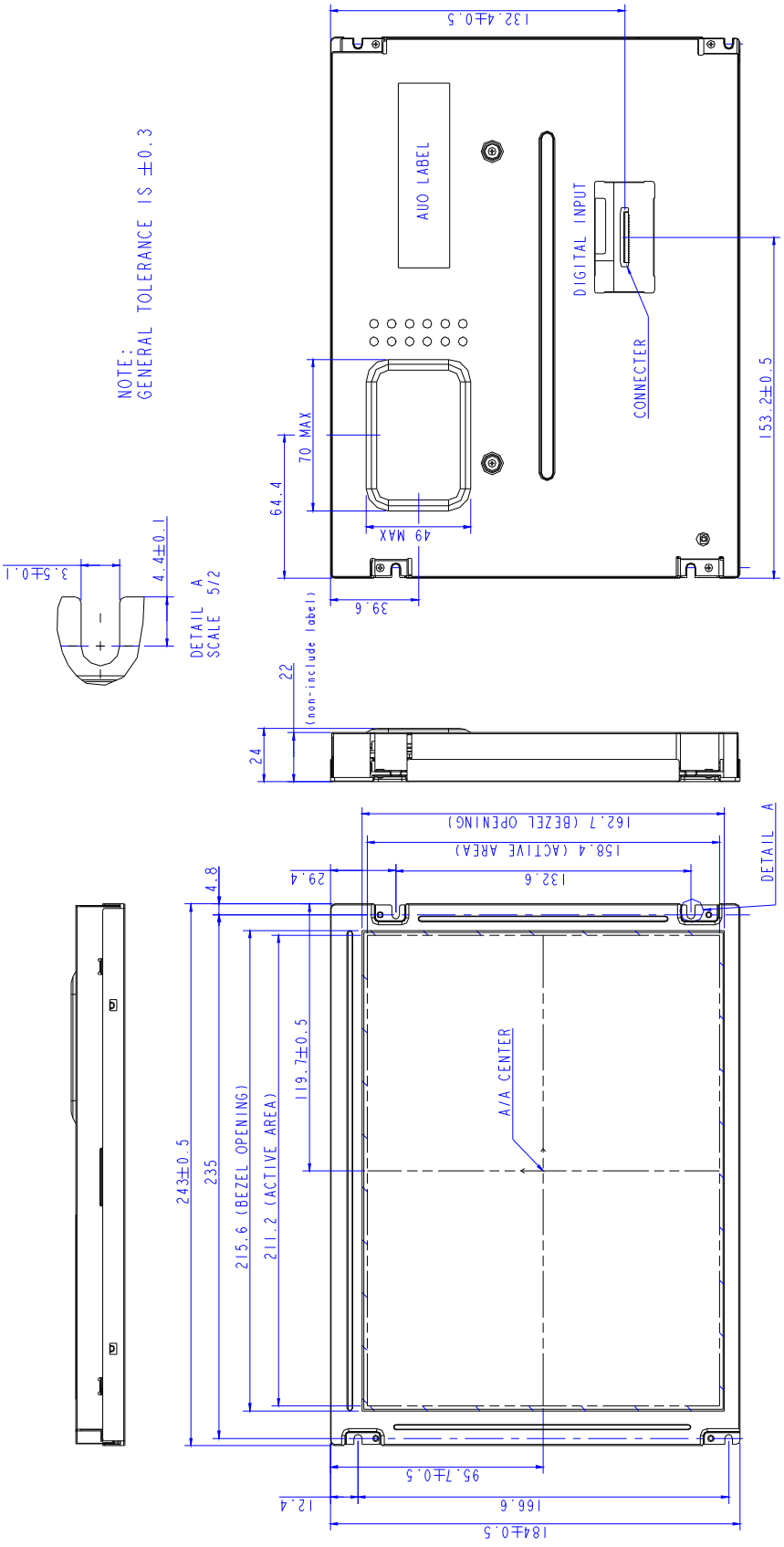


Fig.1 Outline dimension of TFT-LCD module