Product Specification

AU OPTRONICS CORPORATION

B133EW01 V4

( ) Preliminary Specifications
(V) Final Specifications

Module	13.3” WXGA Color TFT-LCD
Model Name	B133EW01 V4
Dell Part No.	XU290

Customer **Date** **Checked & Approved by**	**Approved by** **Date** **Prepared by**
Note: This Specification is subject to change without notice.	NBBU Marketing Division / AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2007/02/14	All	First Edition for Customer		
0.2 2007/04/30	31	Screw hole maximum depth, from side surface =2.5mm	Screw hole maximum depth, from side surface =2.0mm	
0.3 2007/05/17	33		Modify EDID content	
0.4 2007/06/01	33		Modify EDID content	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B133EW01 V4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B133EW01 V4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

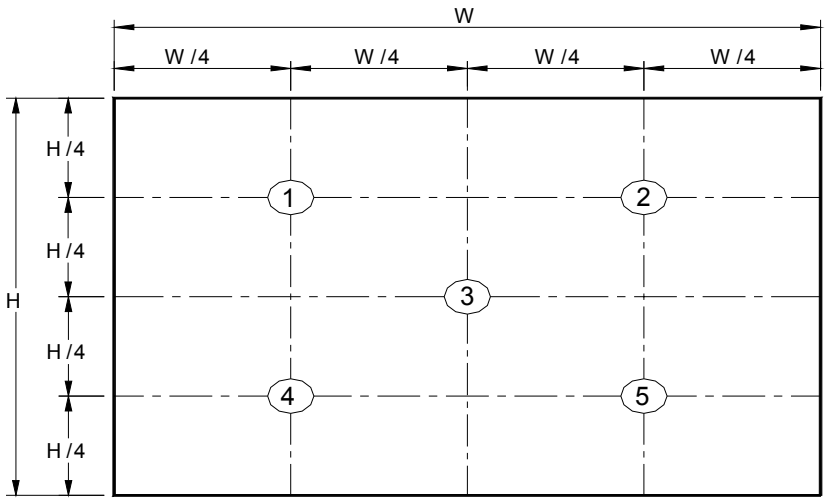
Items	Unit	Specifications
Screen Diagonal	[mm]	337.8 (13.3 W")
Active Area	[mm]	286.08 (H) x 178.8 (V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.2235 x 0.2235
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I_{CCFL}=6.0mA) Note: I_{CCFL} is lamp current	[cd/m^2]	220 typ. (5 points average) 200 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		500 typ
Optical Rise Time/Fall Time	[msec]	16 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	5.2 max.(without inverter)
Weight	[Grams]	365 max.
Physical Size	[mm]	299.5 max. (W) x 195.5 max. (H) x 5.5
Electrical Interface		1 channel LVDS
Surface Treatment		Glare, Hardness 3H, Reflectance ~4 %
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

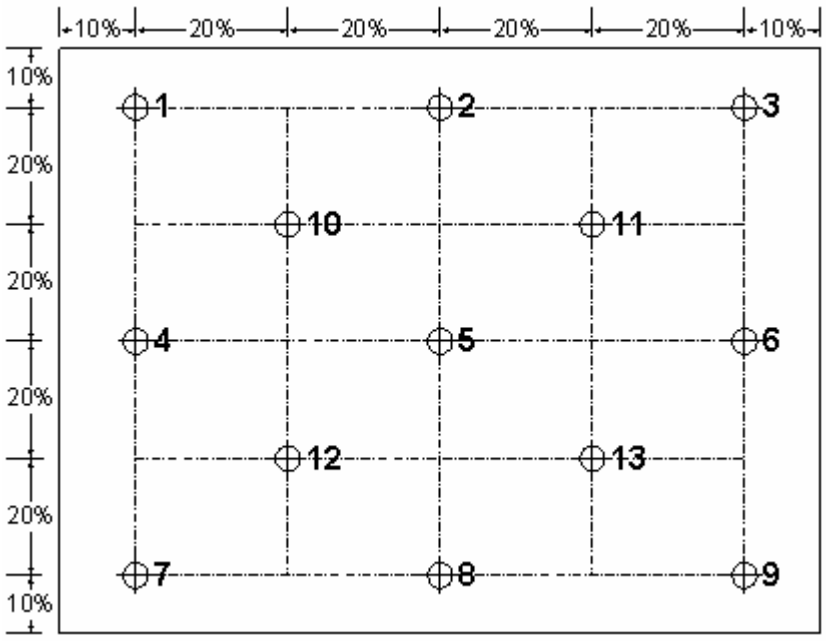
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I_{CCFL}=6.0mA	[cd/m^2]	5 points average	200	220	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10	40	45	-	8
	[degree]	(Left)	40	45	-	
	[degree]	Vertical (Upper) CR = 10	15	25	-	
	[degree]	(Lower)	30	35	-	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			1.50	2
CR: Contrast Ratio			300	500	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.580	0.600	2,8
		Red y	0.320	0.340	0.360	
		Green x	0.290	0.310	0.330	
		Green y	0.530	0.550	0.570	
		Blue x	0.135	0.155	0.175	
		Blue y	0.135	0.155	0.175	
		White x	0.293	0.313	0.333	
		White y	0.309	0.329	0.349	

Note 1: 5 points position (Display area : 286.08 (H) x 178.8 (V)mm)



Note 2: 13 points position



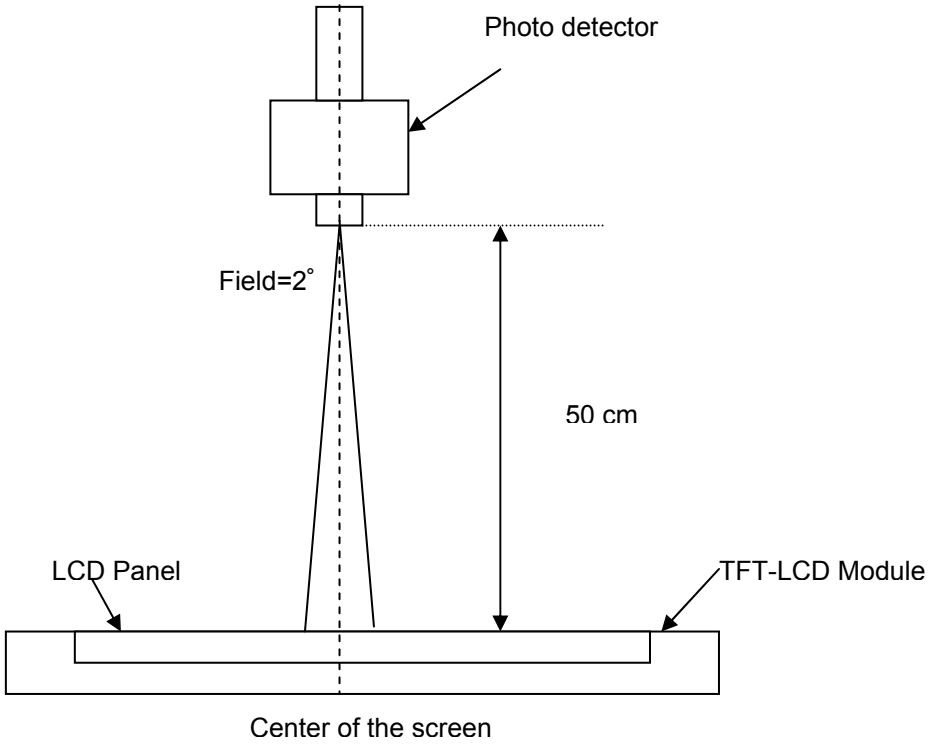
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

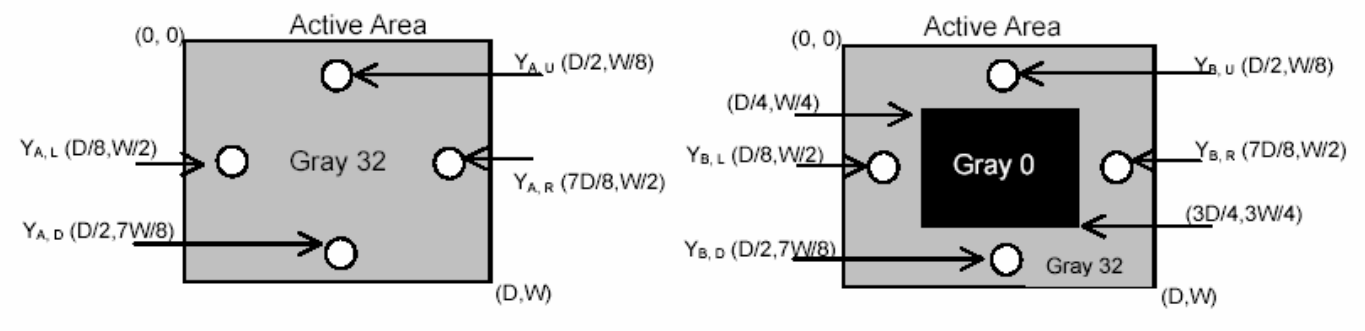
Note 7： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A × 100 (%)

Where

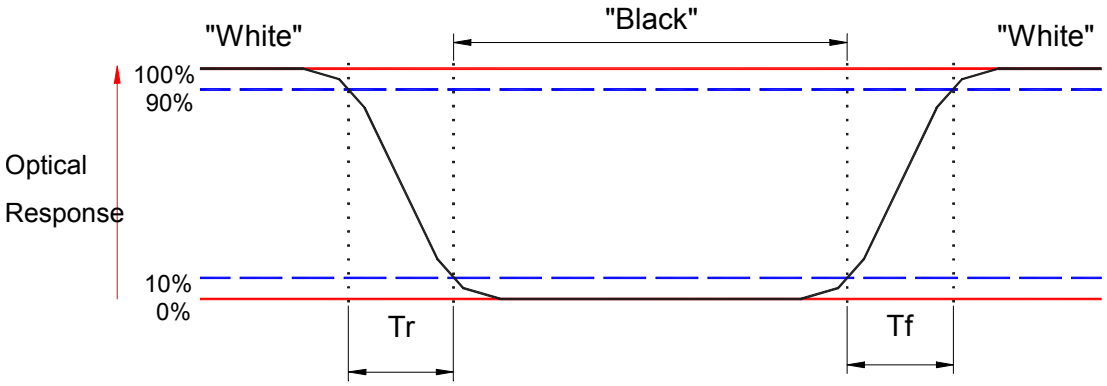
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



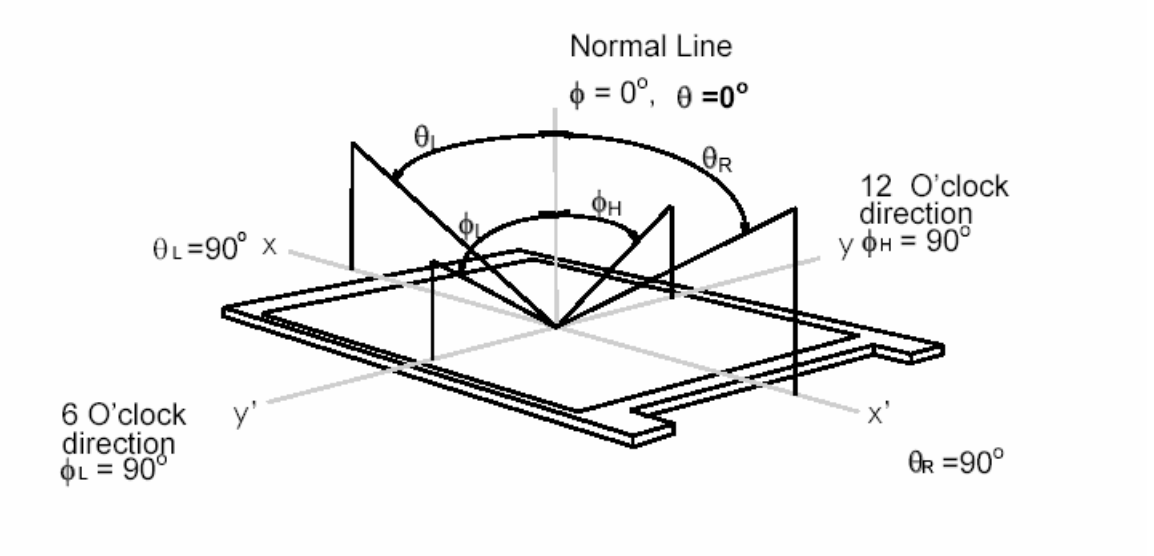
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



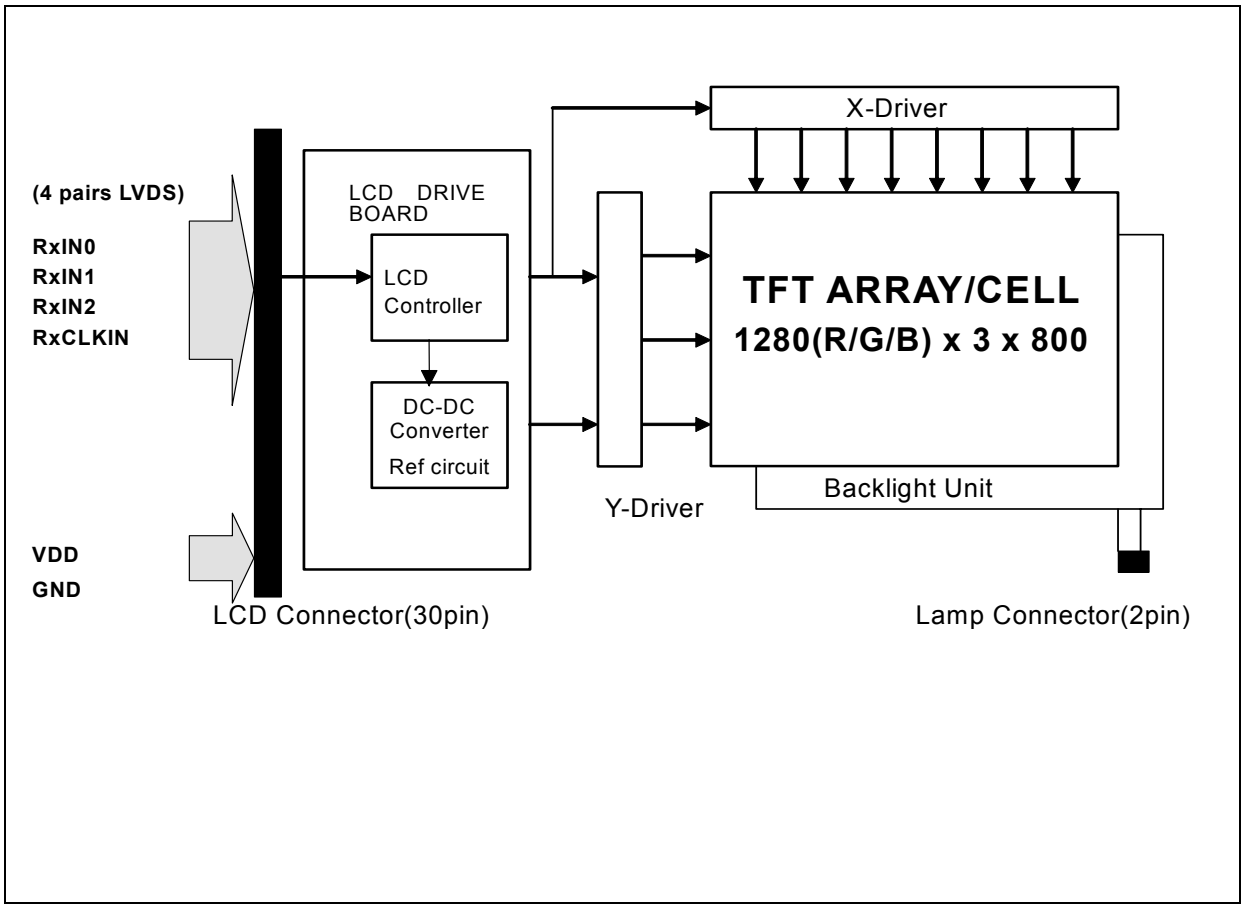
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 13. 3inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

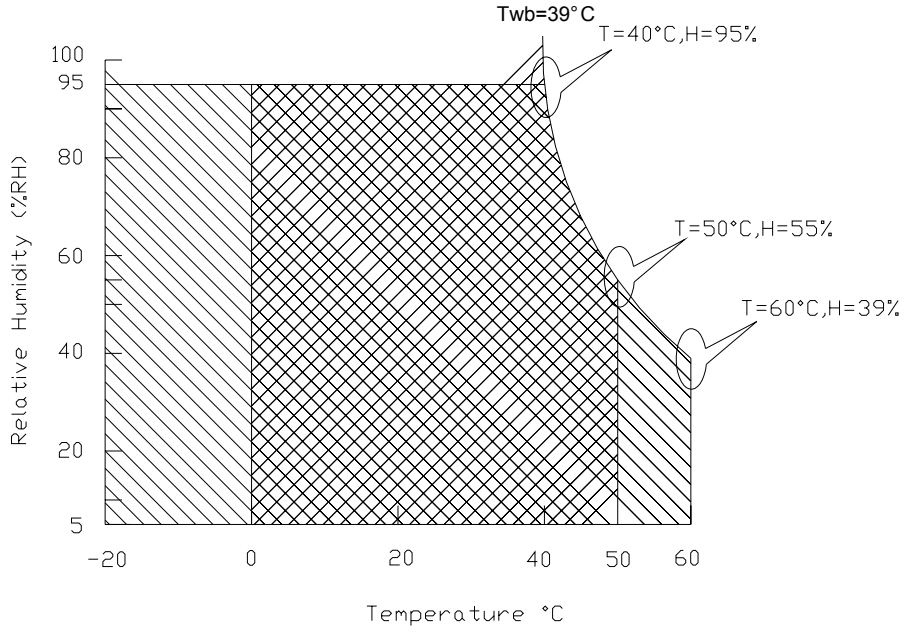
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

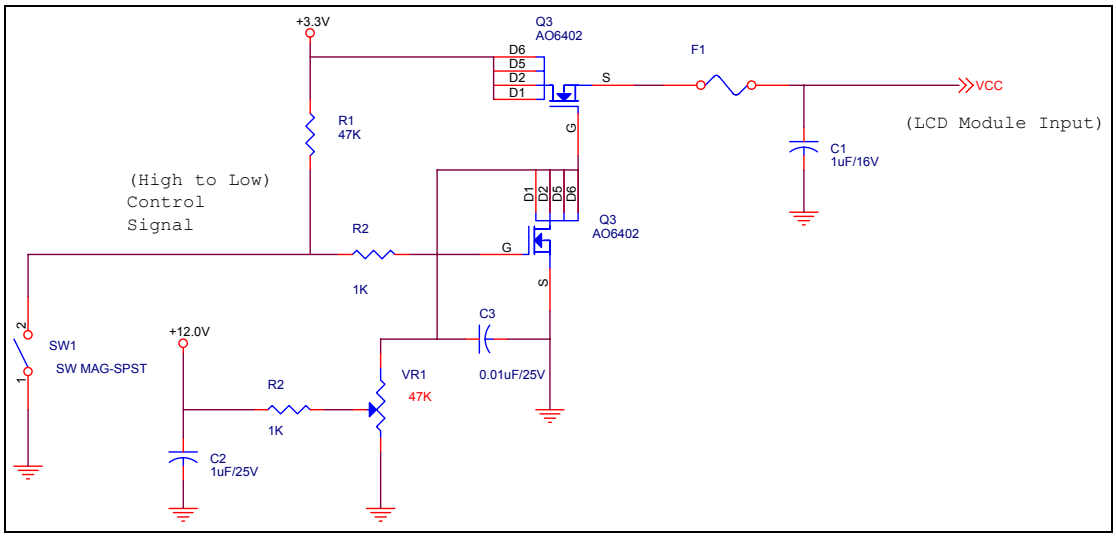
5.1.1 Power Specification

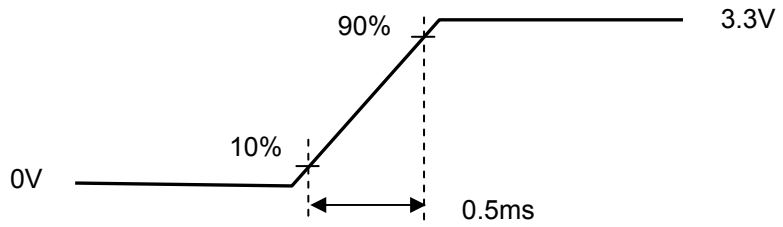
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.0	[Watt]	Note 1
IDD	IDD Current		200	2500	[mA]	Note 1
IRush	Inrush Current			1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Patterm

Note 2：Measure Condition





Vin rising time

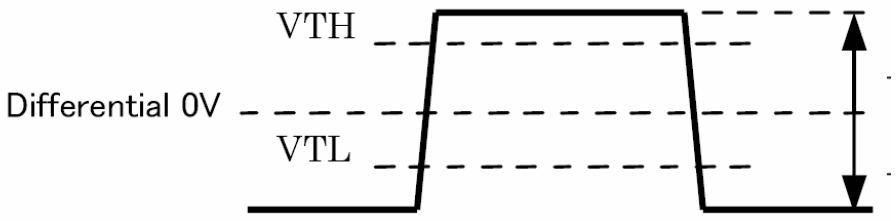
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.0	1.5	[V]

Note: LVDS Differential Voltage



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	200	220	-	[cd/m^2]	(Ta=25℃)
CCFL current(I_{CCFL})	2.0	6.0	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(F_{CCFL})	45	62	70	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1315			[Volt] rms	(Ta= 0℃) Note 5
CCFL Ignition Voltage(Vs)	1095			[Volt] rms	(Ta= 25℃) Note 5
CCFL Voltage (Reference) (VCCFL)	608	640	672	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (P_{CCFL})	-	3.85	4.2	[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

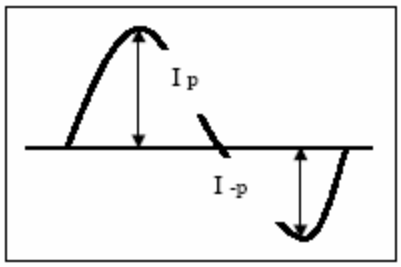
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should bewithin √2 ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

5.3 Inverter charateristic

5.3.1 Foxconn inverter (with Maxim IC)

Electrical Characteristics : Vin= 7.5V~21V

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	INV_SRC	-	7.5	14.0	21.0	V
2	Input Voltage	5VALW	-	4.75	-	5.20	V
3	Input Current	Iin	Vin=14.0V, SMBus=FFH	-	0.38	-	A
4	Input Power	Pin	Vin=14.0V, SMBus=FFH	-	5.2	-	W
5	SMBus Mode Brightness Adjust	SMB_DAT	Min. output: 00H Max. output: FFH	00	-	FF	Hex.
6	DPST mode (System side PWM input)	PWM(Hz)	-	-	10	-	KHz
		PWM Voltage	-	3.135	3.30	3.465	V
		Signal intensity	-	00	-	FF	Hex
7	Output Voltage	Vout	Max. output	-	640	-	Vrms
8	Output Current	Iout (Min)	Ta=25℃, after running 30 min.	1.4	1.7	2.0	mArms
		Iout (Max)		5.7	6.0	6.30	mArms
9	Frequency	Freq	Max. output	45	55	65	KHz
10	Output Power	Pout	Vin=14.0V, SMBus=FFH	-	3.84	-	W
11	Burst Mode Frequency	f_B		200	210	220	Hz
13	Open Lamp Voltage(2)	Vopen	No Load	1400	-	1800	Vrms
14	Striking Time	Ts	No Load	0.6	-	1.4	Sec
15	Efficiency	η	Vin=7.5V, Max. output, Load=100K	-	80	-	%
16	Start –up time			-	-	0.1	Sec

5.3.2 Sumida inverter (with Maxim IC)

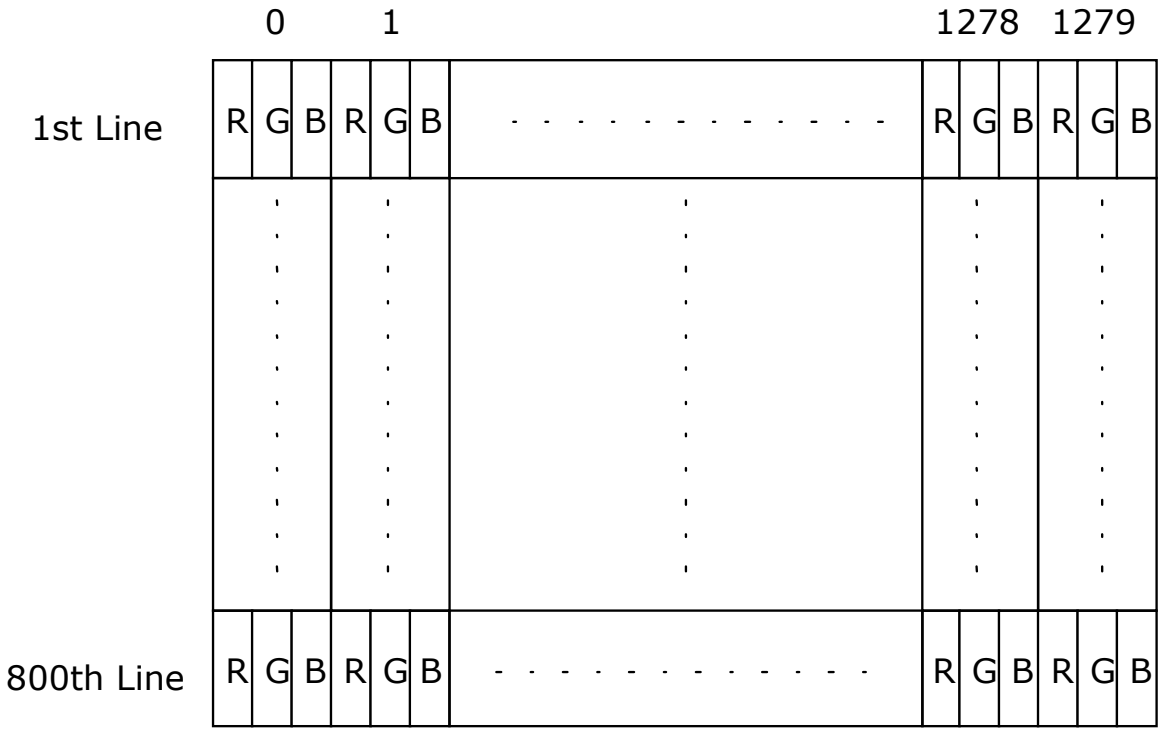
Electrical Characteristics: Vin= 7.5V~21V

	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	Vin		7.5	14.4	21	V
2	Input Current	Iin	Vin=7.5V,SMData=FFH Vin=7.5V,PWM=100%	560	620	680	mA
3	Input Power	Pin	Vin=7.5V,SMData=FFH Vin=7.5V,PWM=100%	---	4.65	---	W
4	Input Signal Level for 5VSUS,5VALW			4.75	5	5.25	V
5	Backlight Adjust(Lamp current control)	SMData	control by SMBus	00H	--	FFH	
6	Output Voltage	Vout	Vin=7.5V,SMData=FFH Vin=7.5V,PWM=100%	576	640	704	Vrms
7	Output current	Iout(Min)	Vin(7.5~21V)SMB_DATA=00H,PWM=10%, Ta=25℃,after running 30 min	1.4	1.7	2.0	mArms
		Iout(Max)	Vin(7.5~21V)SMB_DATA=FFH,PWM=100%, Ta=25℃,after running 30 min	5.7	6.0	6.3	mArms
8	Min currect duty cycle	% duty cycle	Vin=7.5~21V,SMData=00H Vin=7.5V,PWM=100%	6	10	14	%
9	Frequency	Freq	Vin=7.5~21V	48	57	63	KHz
10	Output power	Pout	Vin=21V,SMData=FFH Vin=21V,PWM=100%	---	3.9	---	W
11	Open lamp voltage	Vopen	No load	1400	--	1800	Vrms
12	Striking time	Ts	Vin=7.5~21V	0.6	1	1.4	Sec
13	Efficiency	η	Vin=7.5V,Iout=Max. Load=120KΩ//12PF TO GND	80	--	--	%

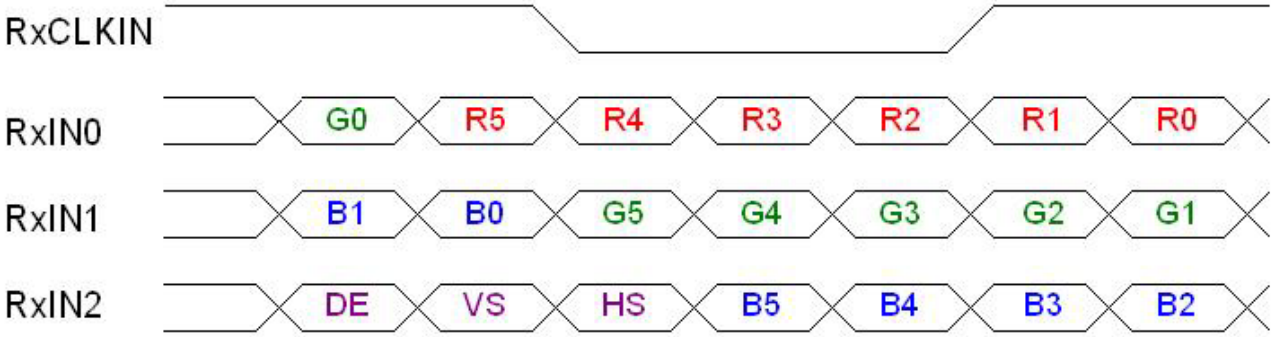
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

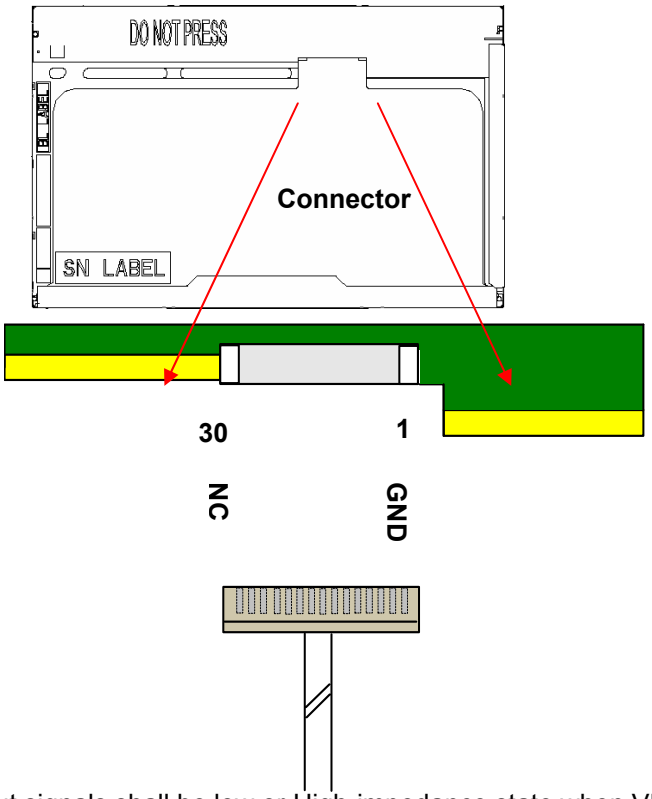
Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V_{EDID}	+3.3V EDID Power
5	NC	No Connection (Reserve for AUO test)
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	GND	Ground
21	NC	No Connection (Reserve for AUO test)
22	NC	No Connection (Reserve for AUO test)
23	NC	No Connection (Reserve for AUO test)
24	NC	No Connection (Reserve for AUO test)
25	NC	No Connection (Reserve for AUO test)
26	NC	No Connection (Reserve for AUO test)
27	NC	No Connection (Reserve for AUO test)
28	NC	No Connection (Reserve for AUO test)
29	NC	No Connection (Reserve for AUO test)
30	NC	No Connection (Reserve for AUO test)

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

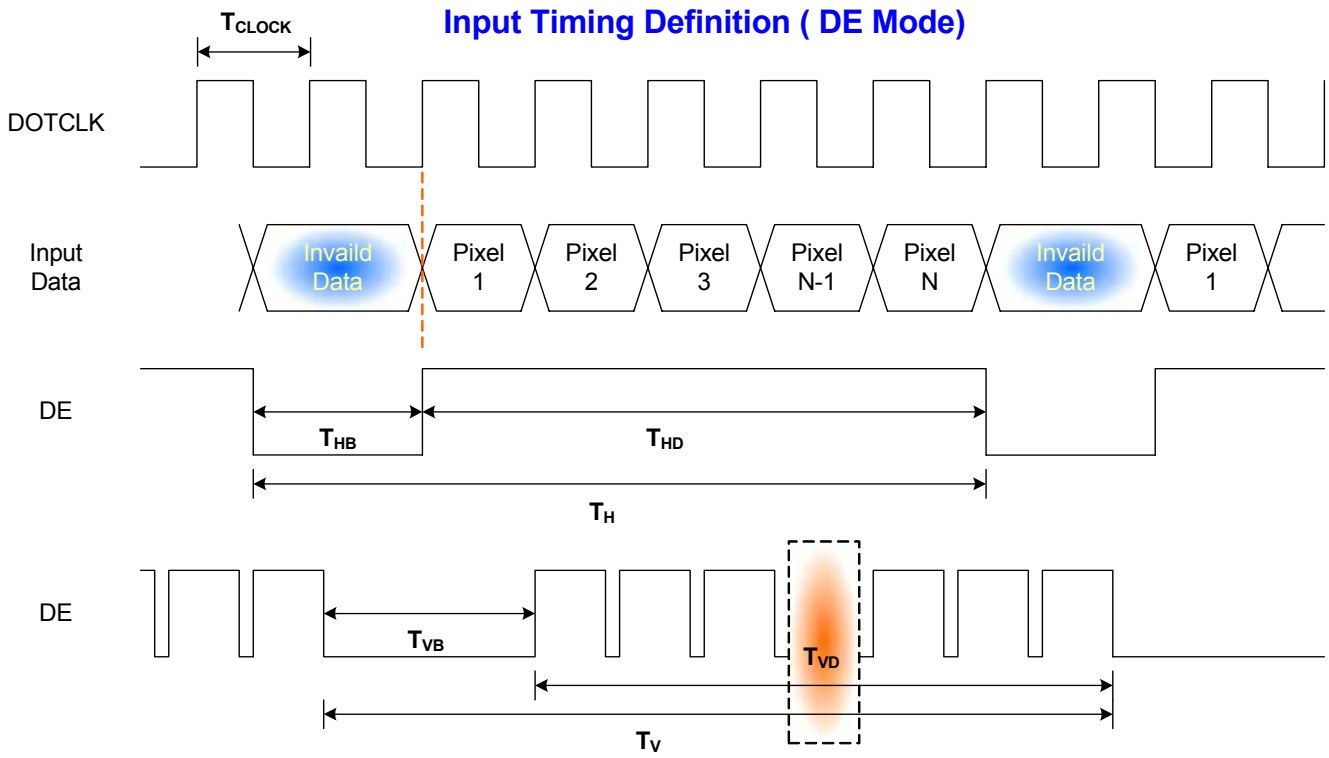
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		1/ T_{Clock}	50	71.1	80	MHz
Vertical Section	Period	T_V	803	823	832	T_{Line}
	Active	T_{VD}	-	800	-	
	Blanking	T_{VB}	3	23	32	
Horizontal Section	Period	T_H	1302	1440	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	160	420	

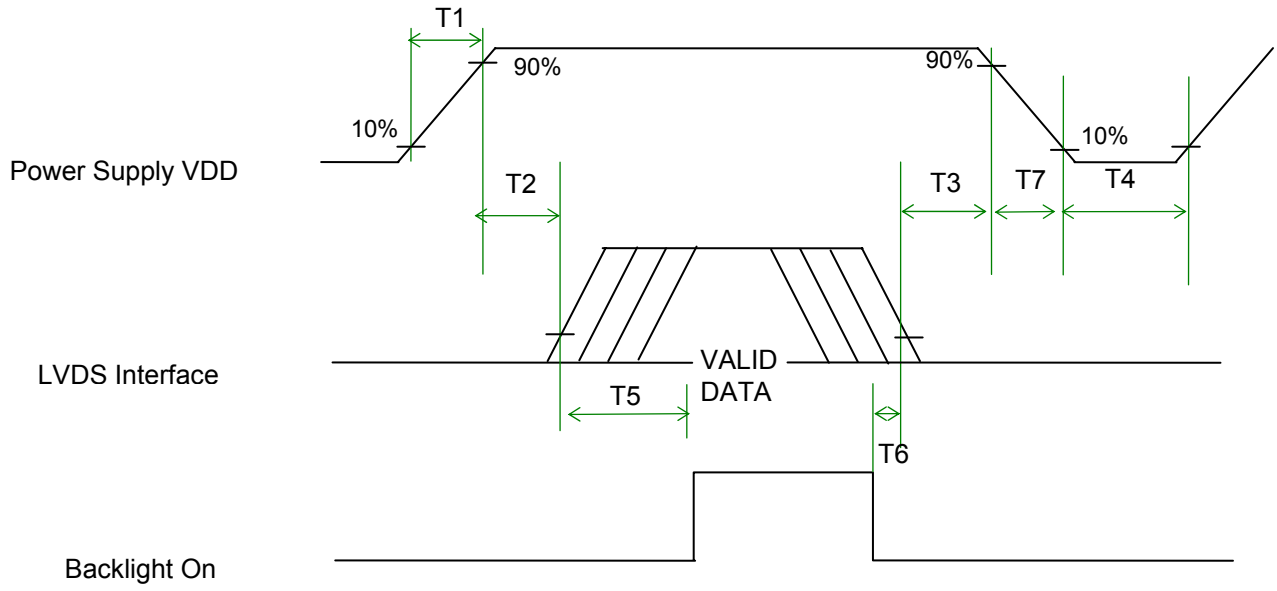
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	HRS or compatible
Type / Part Number	HRS,MDF76KBW-30S-1H or equivalent
Mating Housing/Part Number	MDF76KBW-30S-1H or equivalent – Locking type connector

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G , sine wave
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 200 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/90%,300Hr	
High Temperature Operation	60℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hr	
On/Off Test	25℃, ON/30 sec. OFF/30sec., 10,000 cycles)	
Hot Storage	60℃/35% RH ,250 hours	
Cold Storage	-20℃/50% RH ,250 hours	
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles	
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	200G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Sine-wave vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

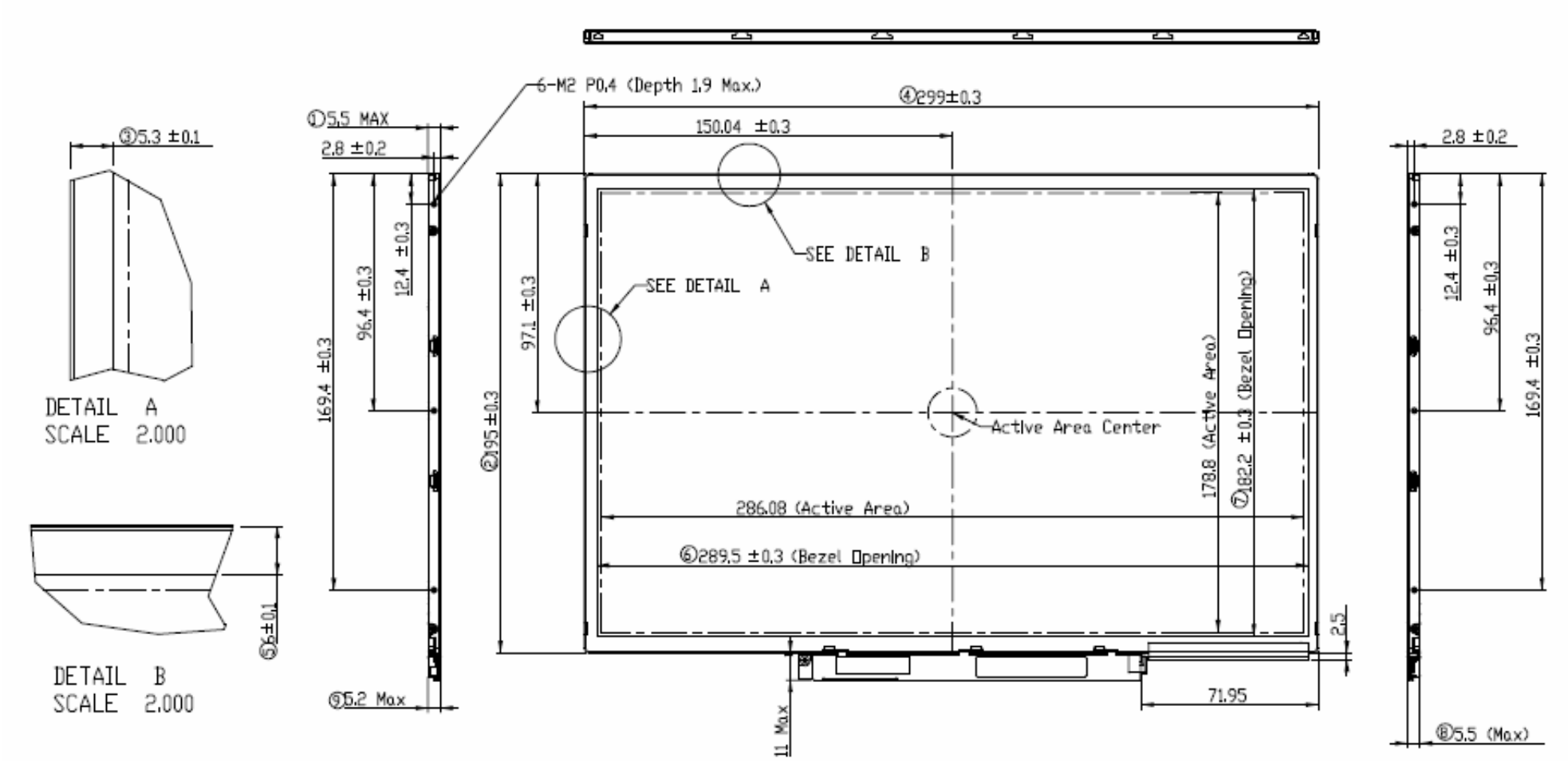
. Self-recoverable. No hardware failures.

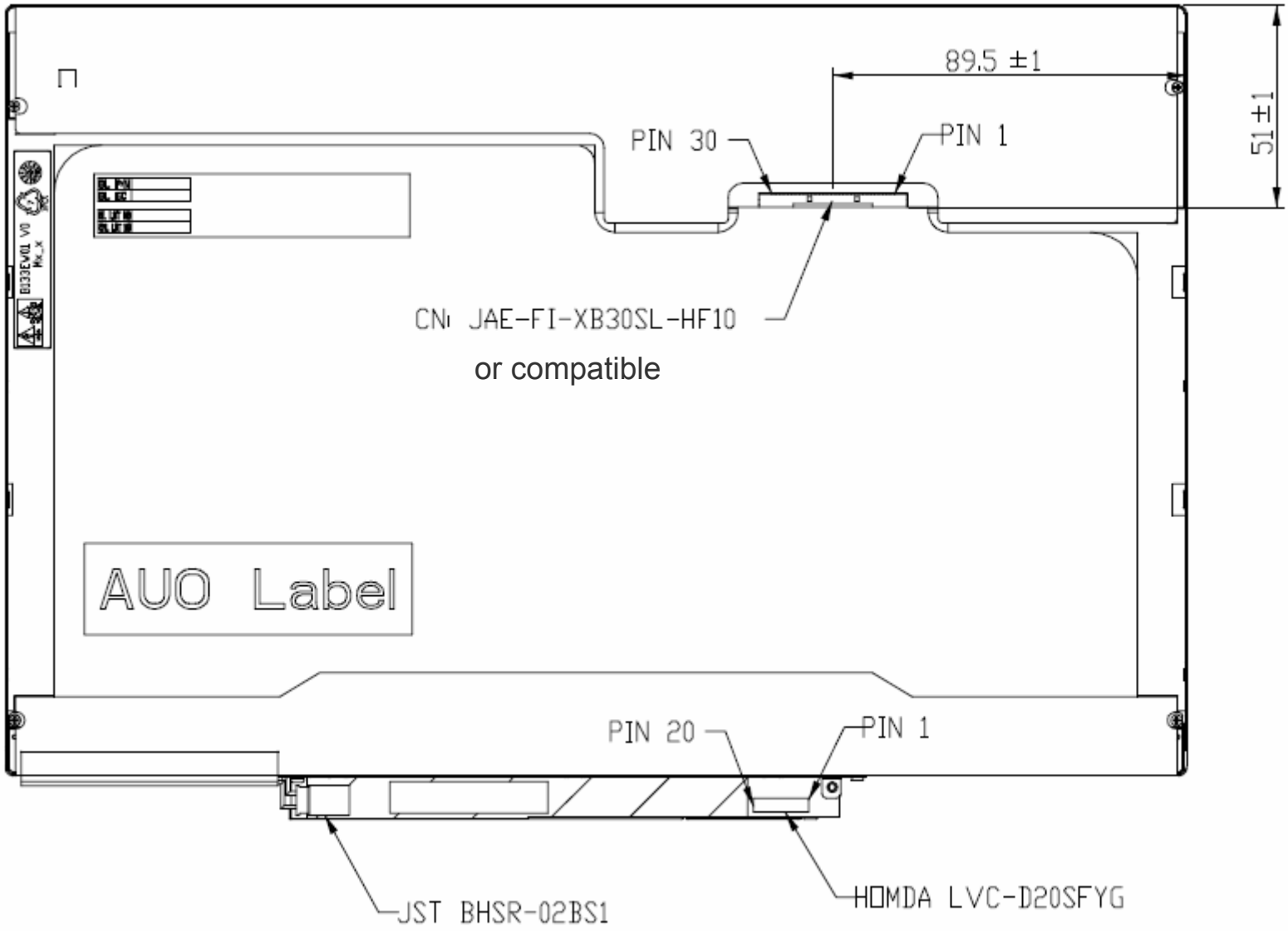
Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

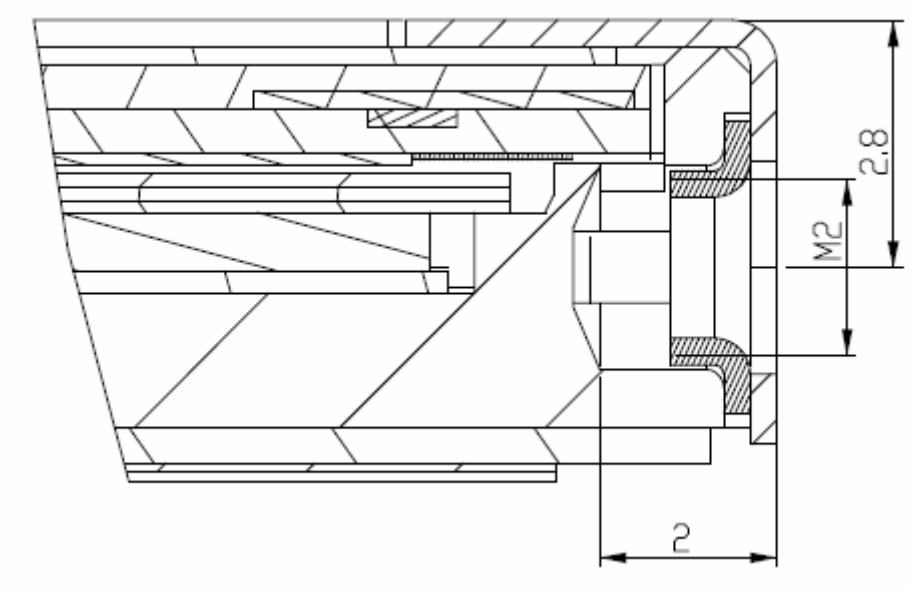



89.5 ±1
51±1
PIN 30
PIN 1
CN1 JAE-FI-XB30SL-HF10
or compatible
AUO Label
PIN 20
PIN 1
JST BHSR-02BS1
HOMDA LVC-D20SFYG

10.2 Screw Hole Depth and Center Position

Screw hole maximum depth, from side surface =2.0 mm (See drawing)

Screw hole center location, from front surface = 2.8 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.1 kgf-cm



11. Shipping and Package

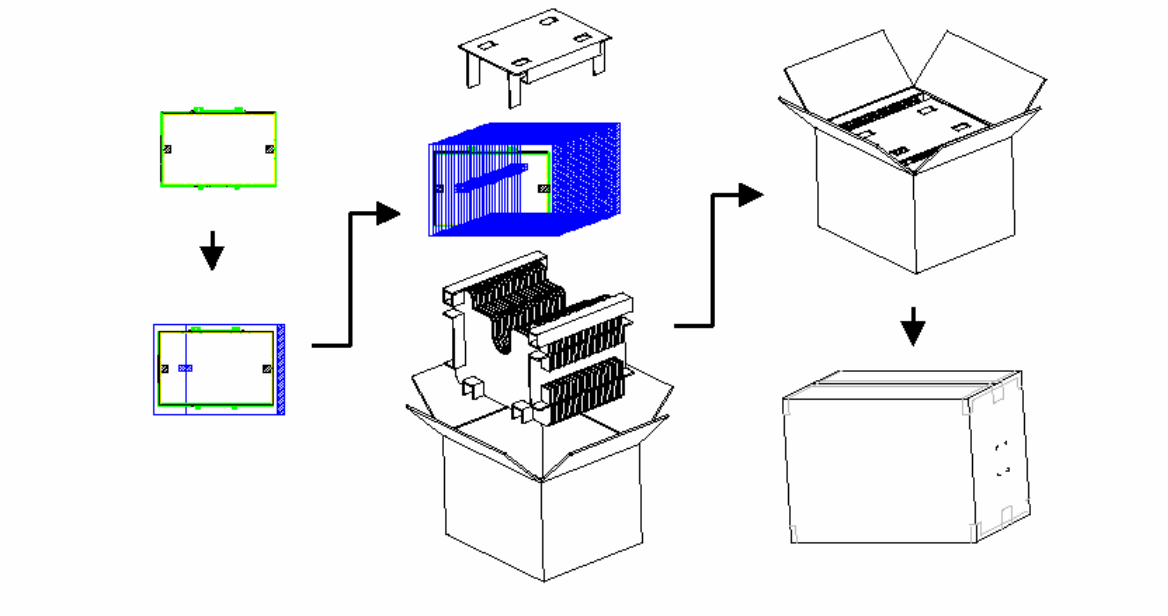
11.1 Shipping Label Format

Note 1:

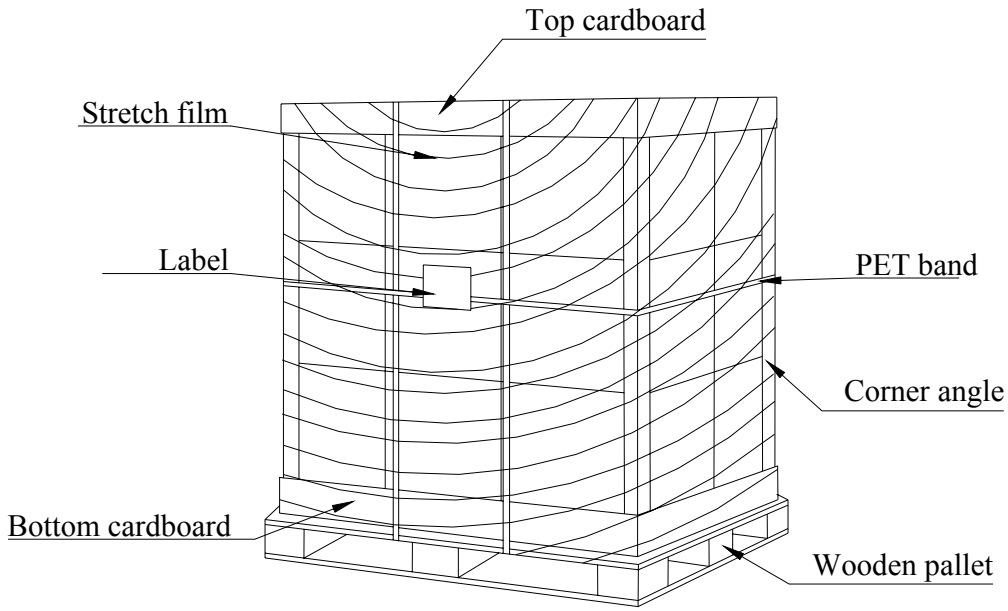
IC Combination	Inverter	Control Code	H/W
Toshiba/Toshiba (gate/source)	Foxconn	1AXXX	1A
Toshiba/Toshiba (gate/source)	Sumida	3AXXX	3A

11.2. Carton package

The outside dimension of carton is 483 mm x378 mm x 310 mm



11.3 Shipping package of palletizing



12. Appendix: EDID description

	Byte (hex)	Field Name and Comments	Value (hex)
Header	0	Header	00
	1	Header	FF
	2	Header	FF
	3	Header	FF
	4	Header	FF
	5	Header	FF
	6	Header	FF
	7	Header	00
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06
	9	EISA manufacture code (Compressed ASCII)	AF
	0A	Panel Supplier Reserved – Product Code	24
	0B	Panel Supplier Reserved – Product Code	14
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00
	10	Week of manufacture	01
	11	Year of manufacture	11
	12	EDID structure version # = 1	01
	13	EDID revision # = 3	03
Display Parameters	14	Video I/P definition = Digital I/P (80h)	80
	15	Max H image size = 29 cm(Rounded to cm)	1D
	16	Max V image size = 18 cm(Rounded to cm)	12
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78
	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	87
	1A	Blue/White Low bit (BxBy/WxWy)	F5
	1B	Red X Rx = 0.580	94
	1C	Red Y Ry = 0.340	57
	1D	Green X Rx = 0.310	4F
	1E	Green Y Ry = 0.550	8C
	1F	Blue X Rx = 0.155	27
	20	Blue Y Ry = 0.155	27

	21	White X Rx = 0.313	50
	22	White Y Ry = 0.329	54
Established Timings	23	Established timings 1 (00h if not used)	00
	24	Established timings 2 (00h if not used)	00
	25	Manufacturer's timings (00h if not used)	00
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01
	27	Standard timing ID1 (01h if not used)	01
	28	Standard timing ID2 (01h if not used)	01
	29	Standard timing ID2 (01h if not used)	01
	2A	Standard timing ID3 (01h if not used)	01
	2B	Standard timing ID3 (01h if not used)	01
	2C	Standard timing ID4 (01h if not used)	01
	2D	Standard timing ID4 (01h if not used)	01
	2E	Standard timing ID5 (01h if not used)	01
	2F	Standard timing ID5 (01h if not used)	01
	30	Standard timing ID6 (01h if not used)	01
	31	Standard timing ID6 (01h if not used)	01
	32	Standard timing ID7 (01h if not used)	01
	33	Standard timing ID7 (01h if not used)	01
	34	Standard timing ID8 (01h if not used)	01
	35	Standard timing ID8 (01h if not used)	01
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	EE
	37	Pixel Clock/10,000 (MSB)	1B
	38	Horizontal Active = 1280 pixels (lower 8 bits)	00
	39	Horizontal Blanking (Thbp) = 160 pixels (lower 8 bits)	A8
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50
	3B	Vertical Active = 800 lines	20
	3C	Vertical Blanking (Tvbp) = 23 lines (DE Blanking typ. for DE only panels)	17
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
	3E	Horizontal Sync, Offset (Thfp) = 48 pixels	30
	3F	Horizontal Sync, Pulse Width = 32 pixels	20
	40	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 6 lines	36
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	42	Horizontal Image Size =286.8 mm	22
	43	Vertical image Size = 178.8 mm	B4

	44	Horizontal Image Size / Vertical image size	10
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00
	46	Vertical Border = 0 (Zero for Notebook LCD)	00
	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, **DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.**	19
Timing Descripter #2	48	Pixel Clock/10,000 (LSB)	EE
	49	Pixel Clock/10,000 (MSB)	1B
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	00
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	A8
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50
	4D	Vertical Active = xxxx lines	20
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	17
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30
	51	Horizontal Sync, Pulse Width = xxxx pixels	20
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00
	54	Horizontal Image Size =xxx mm	22
	55	Vertical image Size = xxx mm	B4
	56	Horizontal Image Size / Vertical image size	10
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00
	58	Vertical Border = 0 (Zero for Notebook LCD)	00
	59	Module "A" Revision = 00 Example: 00, 01, 02, 03, etc.	00
Timing Descripter #3 Dell specific information	5A	Flag	00
	5B	Flag	00
	5C	Flag	00
	5D	Dummy Descriptor	FE
	5E	Flag	00
	5F	Dell P/N 1st Character	58
	60	Dell P/N 2nd Character	55
	61	Dell P/N 3rd Character	32
	62	Dell P/N 4th Character	39

	63	Dell P/N 5th Character	30
	64	LCD Supplier EEDID Revision #	00
	65	Manufacturer P/N	42
	66	Manufacturer P/N	31
	67	Manufacturer P/N	33
	68	Manufacturer P/N	33
	69	Manufacturer P/N	45
	6A	Manufacturer P/N	57
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	31
Timing Descripter #4	6C	Flag	00
	6D	Flag	00
	6E	Flag	00
	6F	Data Type Tag:	FE
	70	Flag	00
	71	SMBUS Value = 9.82 nits	23
	72	SMBUS Value = 17.01 nits	32
	73	SMBUS Value = 23.75 nits	3D
	74	SMBUS Value = 30.34 nits	46
	75	SMBUS Value = 59.76 nits	64
	76	SMBUS Value = 99.95 nits	81
	77	SMBUS Value = 160.59 nits	A7
	78	SMBUS Value = 219.49 nits	E5
	79	Number of LVDS receiver chips = 01 (01 or 02)	01
	7A	BIST Enable: Yes	01
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	4E