Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications
( ) Final Specifications

Module	15.4” WXGA+ Color TFT-LCD
Model Name	B154PW02 V1

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by		**Prepared by**	
Note: This Specification is subject to change without notice.		AU Optronics corporation	

Contents

1. Handling Precautions 4
2. General Description 4
2.1 General Specification 5
2.2 Optical Characteristics 6
3. Functional Block Diagram 11
4. Absolute Maximum Ratings 12
4.1 Absolute Ratings of TFT LCD Module 12
4.2 Absolute Ratings of Backlight Unit 12
4.3 Absolute Ratings of Environment 12
5. Electrical characteristics 13
5.1 TFT LCD Module 13
5.2 Backlight Unit 15
6. Signal Characteristic 17
6.1 Pixel Format Image 17
6.2 The input data format 18
6.3 Signal Description/Pin Assignment 19
6.4 Interface Timing 21
7. Connector Description 24
7.1 TFT LCD Module 24
7.2 Backlight Unit 24
7.3 Signal for Lamp connector 24
8. Vibration and Shock Test 25
8.1 Vibration Test 25
8.2 Shock Test Spec: 25
9. Reliability 26
10. Mechanical Characteristics 27
10.1 LCM Outline Dimension 27
11.1 Shipping Label Format 29
11.2. Carton package 30
11.3 Shipping package of palletizing sequence 30
12. Appendix: EDID description 31

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2006/12/25	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B154PW02 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA+

(1440(H) x 900(V)) screen and 262k colors. All input signals are LVDS interface compatible. Inverter of backlight is not included.

B154PW02 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

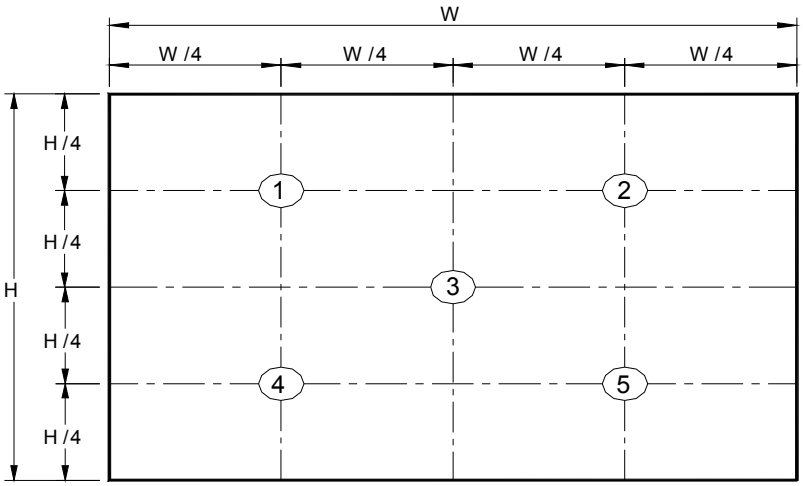
Items	Unit	Specifications
Screen Diagonal	[mm]	391 (15.14W")
Active Area	[mm]	331.2 X 207.0
Pixels H x V		1440 x 3(RGB) x 900
Pixel Pitch	[mm]	0.23025 x 0.23025
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I_{CCFL}=6.0mA) Note: I_{CCFL} is lamp current	[cd/m^2]	250 typ. (5 points average) 210 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ 300 min.
Optical Rise Time/Fall Time	[msec]	4/12 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	6.0 max.(without inverter)
Weight	[Grams]	510 typ. 535max.
Physical Size	[mm]	344.0 typ. x 222.0 typ. x 6.1 max
Electrical Interface		2-channel LVDS
Surface Treatment		Glare, Hardness 3H, Haze 25%
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

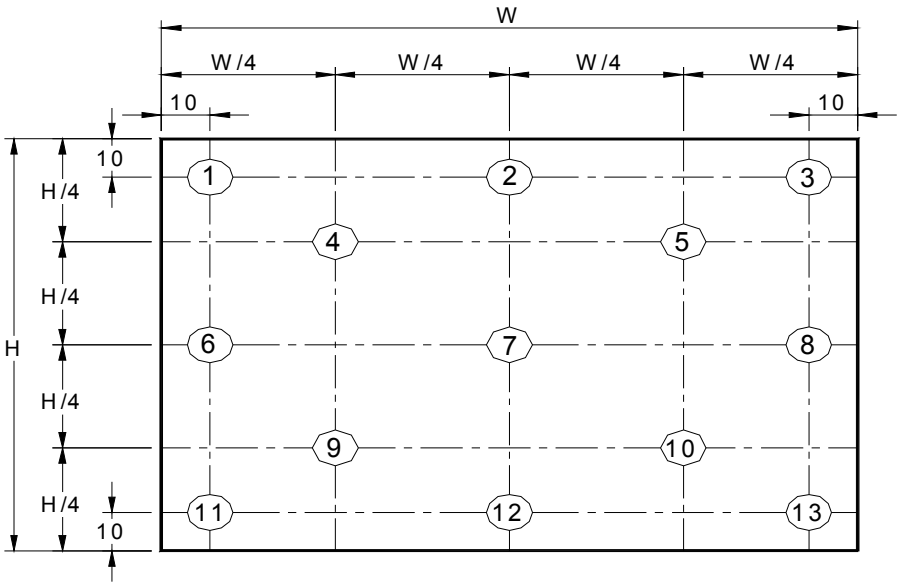
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I_{CCFL}=6.0mA	[cd/m^2]	5 points average	210	250	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right) CR = 10	-	70	-	8
	[degree]	(Left)	-	70	-	
	[degree]	Vertical (Upper) CR = 10	-	60	-	
	[degree]	(Lower)	-	60	-	
Luminance Uniformity		5 Points	-	-	1.25	1
Luminance Uniformity		13 Points	-	-	1.50	2
CR: Contrast Ratio			300	400	-	6
Cross talk	%		-	-	4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling	-	16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.590	0.620	2,8
		Red y	0.315	0.345	0.375	
		Green x	0.285	0.315	0.345	
		Green y	0.520	0.555	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.115	0.145	0.175	
		White x	0.283	0.313	0.343	
		White y	0.289	0.329	0.359	

Note 1: 5 points position (Display area : 331.2mm x 207.0mm)



Note 2: 13 points position



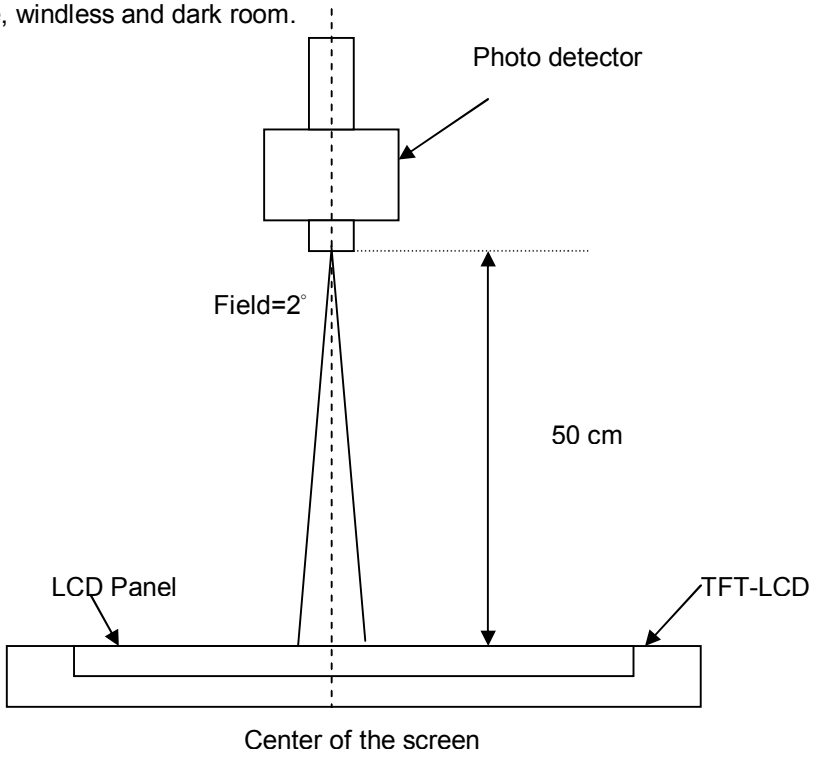
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

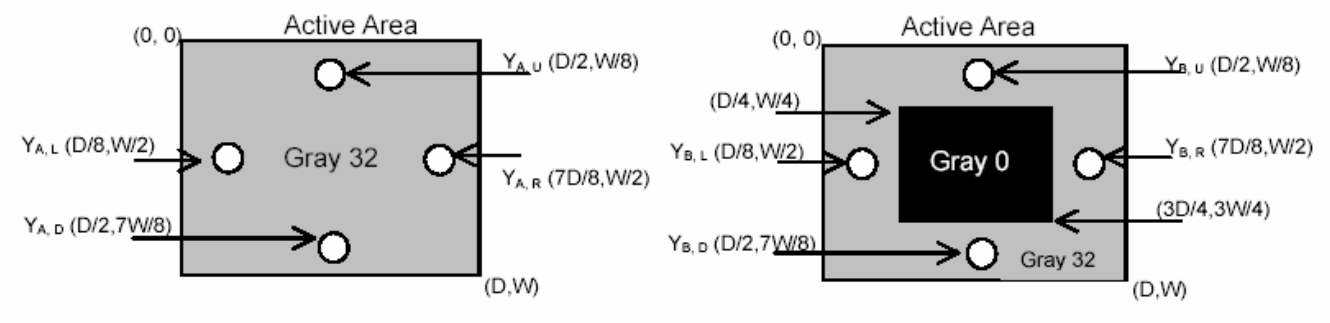
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

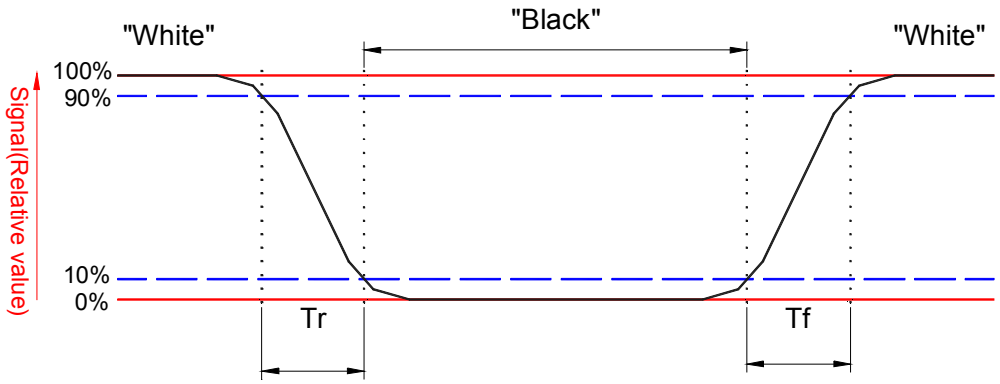
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



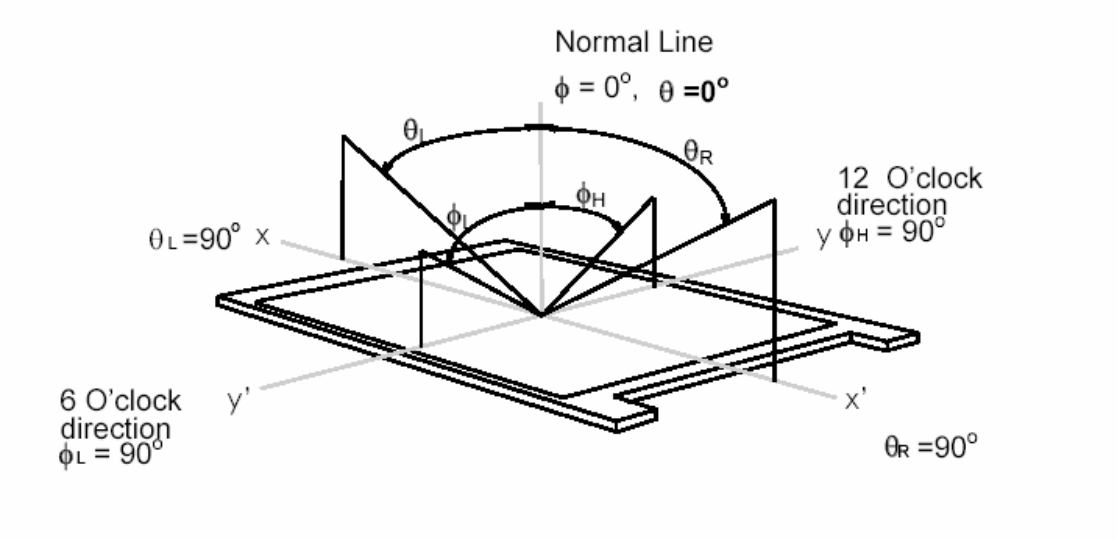
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



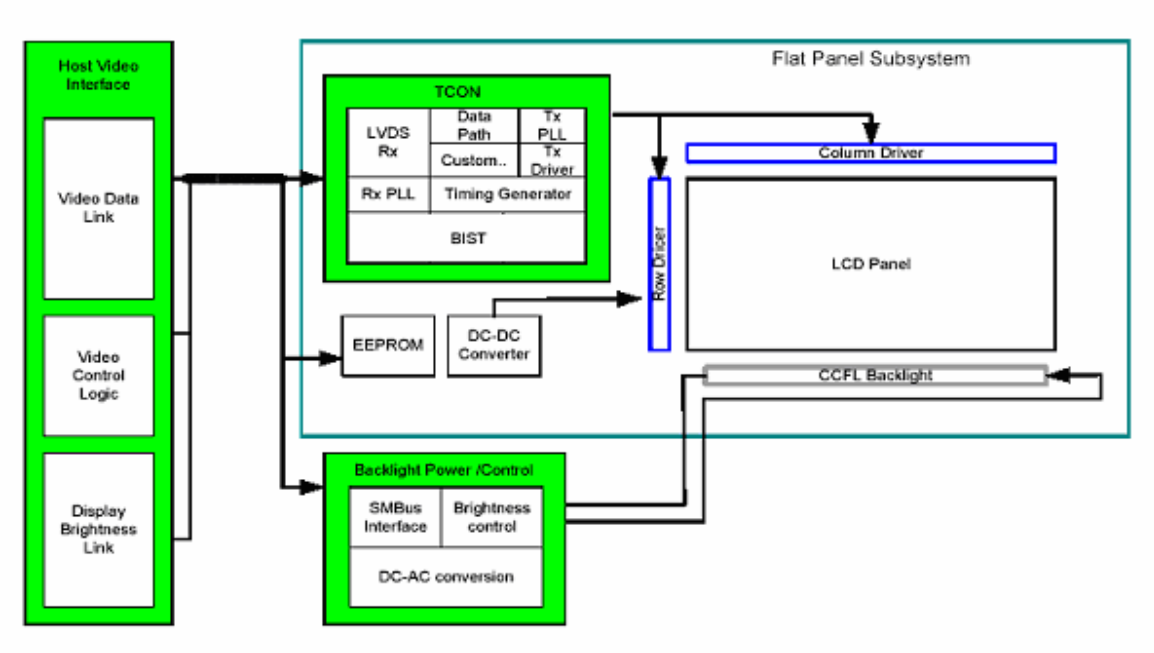
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.4 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

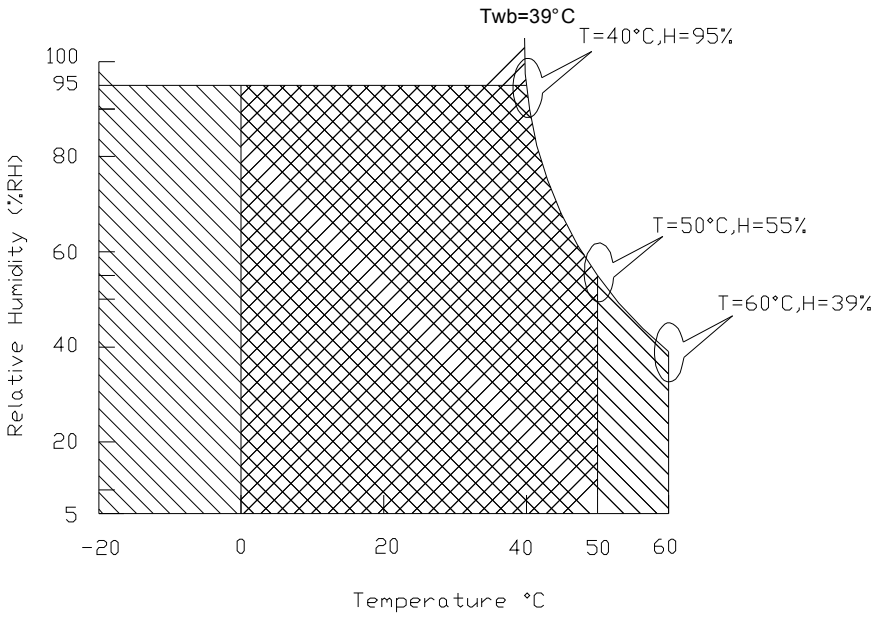
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

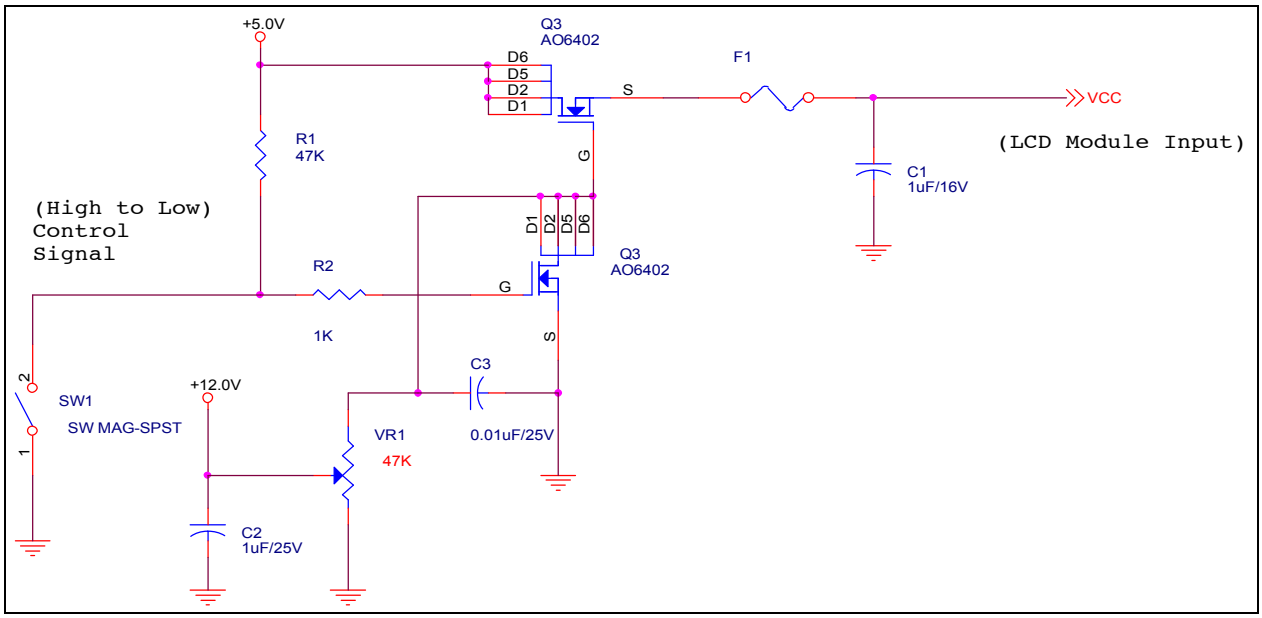
5.1.1 Power Specification

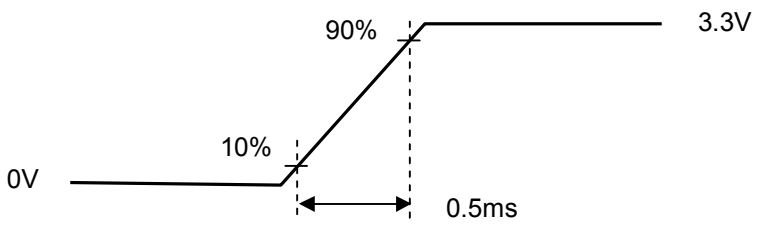
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.5	[Watt]	Note 1
IDD	IDD Current		400	420	[mA]	Note 1
IRush	Inrush Current			2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Patterm

Note 2：Measure Condition





Vin rising time

5.1.2 Signal Electrical Characteristics

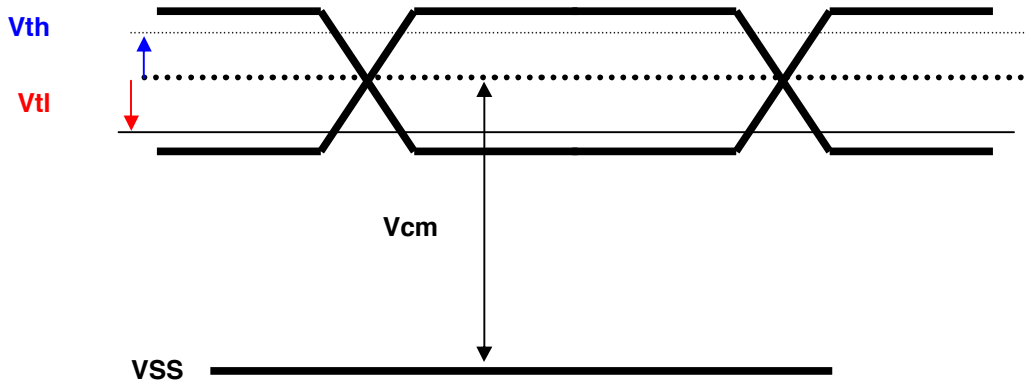
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	210	250	-	[cd/m^2]	(Ta=25℃)
CCFL current(I_{CCFL})	-	6.0	-	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(F_{CCFL})	-	62	-	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1340	-	-	[Volt] rms	(Ta= 0℃) Note 5
CCFL Ignition Voltage(Vs)	1030	-	-	[Volt] rms	(Ta= 25℃) Note 5
CCFL Voltage (Reference) (V_{CCFL})	620	720	910	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (P_{CCFL})	-	4.30	4.70	[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,340 voltage. Lamp units need 1,300 voltage minimum for ignition.

Note 6: Calculator value for reference ($I_{CCFL} \times V_{CCFL} = P_{CCFL}$)

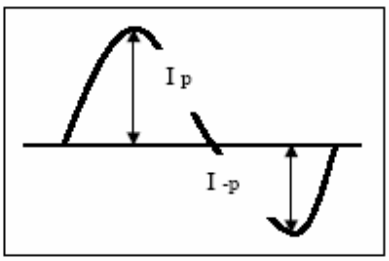
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within $\sqrt{2}$ ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

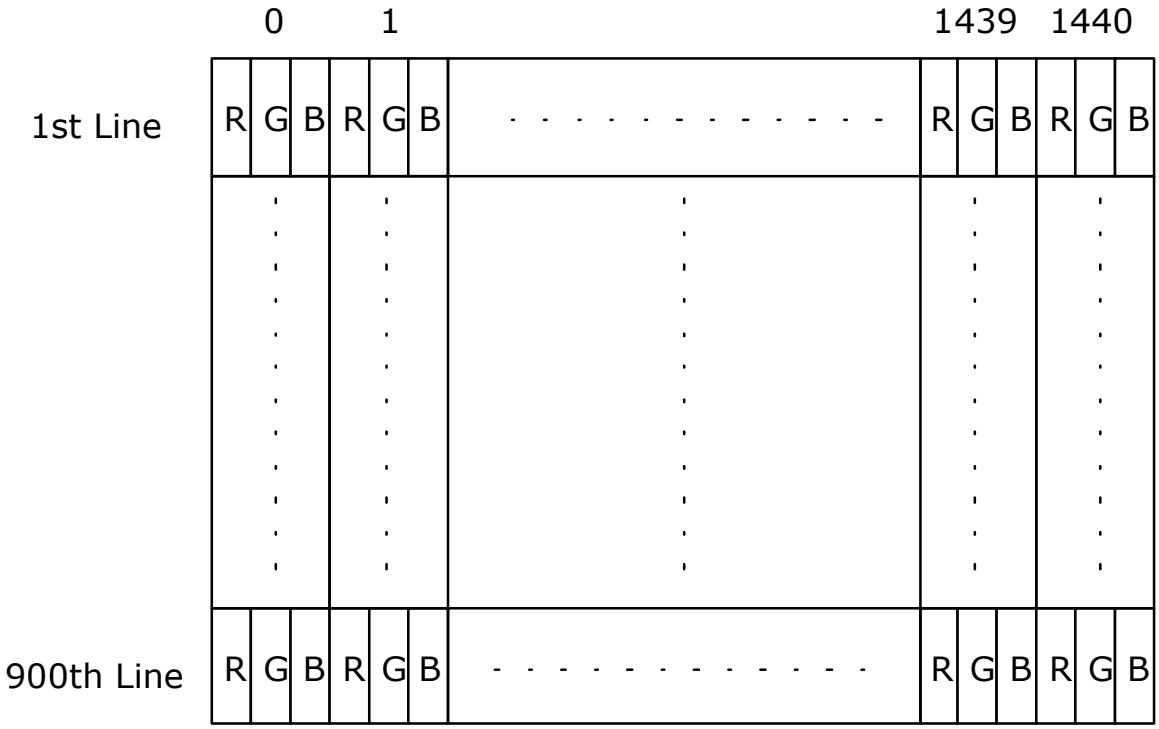
* Distortion rate

I_p (or I_{-p}) / I_{rms}

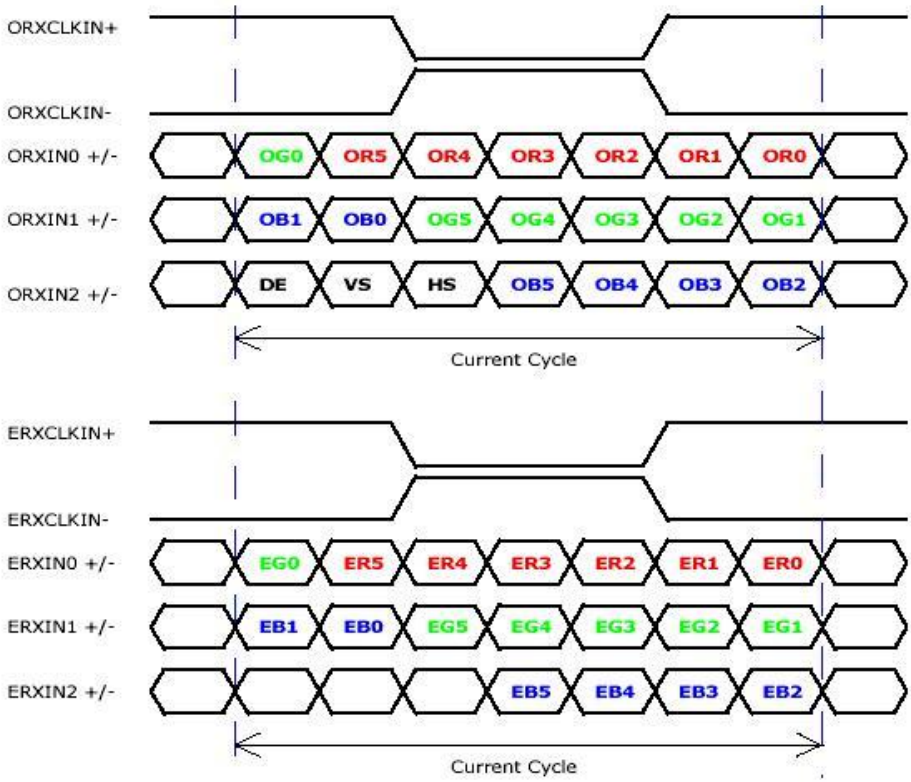
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description
V_{EDID}	+3.3V EDID Power
CLK_{EDID}	EDID Clock Input
$DATA_{EDID}$	EDID Data Input
ORXIN0-, ORXIN0+	Odd LVDS differential data input(ORed0-ORed5, OGreen0)
ORXIN1-, ORXIN1+	Odd LVDS differential data input(OGreen1-OGreen5, OBlue0-OBlue1)
ORXIN2-, ORXIN2+	Odd LVDS differential data input(OBlue2-OBlue5, Hsync, Vsync, DE)
ORXCLKIN-, ORXCLKIN+	Odd LVDS differential clock input
ERXIN0-, ERXIN0+	Even LVDS differential data input(ERed0-ERed5, EGreen0)
ERXIN1-, ERXIN1+	Even LVDS differential data input(EGreen1-EGreen5, EBlue0-EBlue1)
ERXIN2-, ERXIN2+	Even LVDS differential data input(EBlue2-EBlue5)
ERXCLKIN-, ERXCLKIN+	Even LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

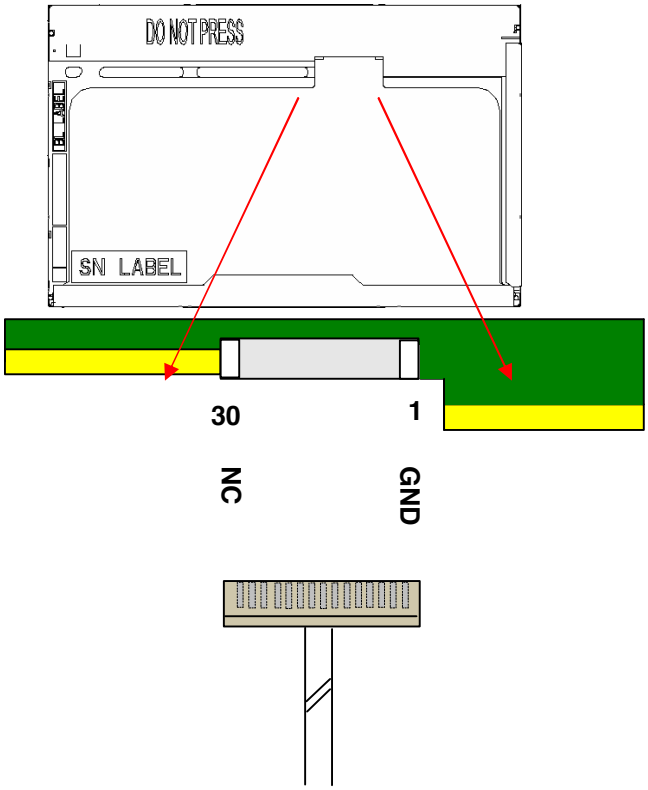
6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN #	SIGNAL NAME	DESCRIPTION
1	VSS	Power Ground
2	VDD	+ 3.3V Power Supply
3	VDD	+ 3.3V Power Supply
4	V_{EDID}	+ 3.3V EDID Power
5	AGING	Aging Mode Power Supply
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	Odd_Rin0-	-LVDS Differential Data Input
9	Odd_Rin0+	+LVDS Differential Data Input
10	VSS	Power Ground
11	Odd_Rin1-	-LVDS Differential Data Input
12	Odd_Rin1+	+LVDS Differential Data Input
13	VSS	Power Ground
14	Odd_Rin2-	-LVDS Differential Data Input
15	Odd_Rin2+	+LVDS Differential Data Input
16	VSS	Power Ground
17	Odd_ClkIN-	-LVDS Differential Clock Input
18	Odd_ClkIN+	+LVDS Differential Clock Input
19	VSS	Power Ground
20	Even_Rin0-	-LVDS Differential Data Input
21	Even_Rin0+	+LVDS Differential Data Input
22	VSS	Power Ground
23	Even_Rin1-	-LVDS Differential Data Input
24	Even_Rin1+	+LVDS Differential Data Input
25	VSS	Power Ground
26	Even_Rin2-	-LVDS Differential Data Input
27	Even_Rin2+	+LVDS Differential Data Input
28	VSS	Power Ground
29	Even_ClkIN-	-LVDS Differential Clock Input
30	Even_ClkIN+	+LVDS Differential Clock Input

.

Note1: Start from right side



6.4 Interface Timing

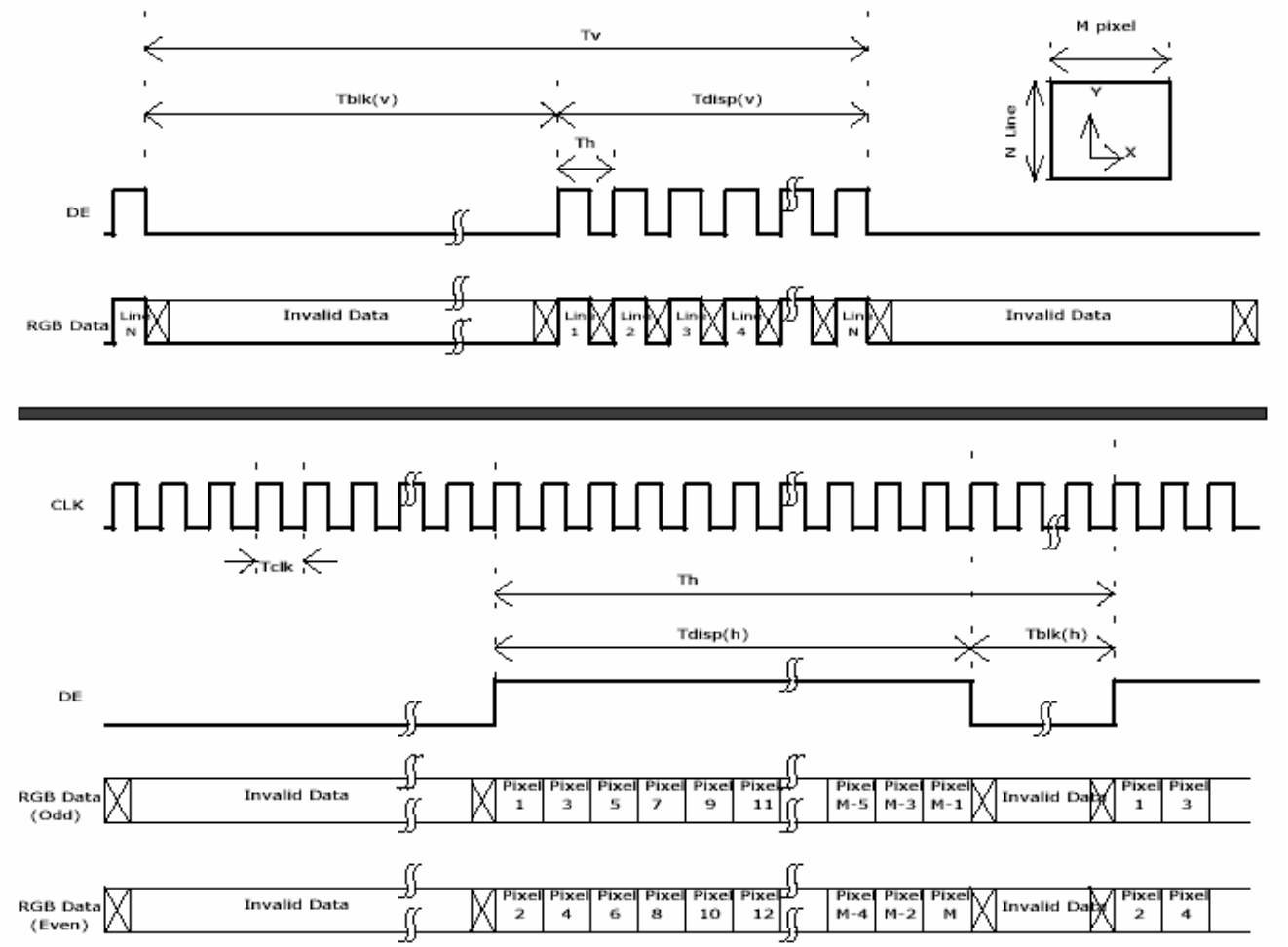
6.4.1 Timing Characteristics

Basically, interface timings should match the 1440X900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		1/ T_{Clock}	50	48.2	60.2	MHz
Vertical Section	Period	T_V	904	912	2048	T_{Line}
	Active	T_{VD}	900	900	900	
	Blanking	T_{VB}	4	12	-	
Horizontal Section	Period	T_H	760	880	1024	T_{Clock}
	Active	T_{HD}	720	720	720	
	Blanking	T_{HB}	40	160	-	

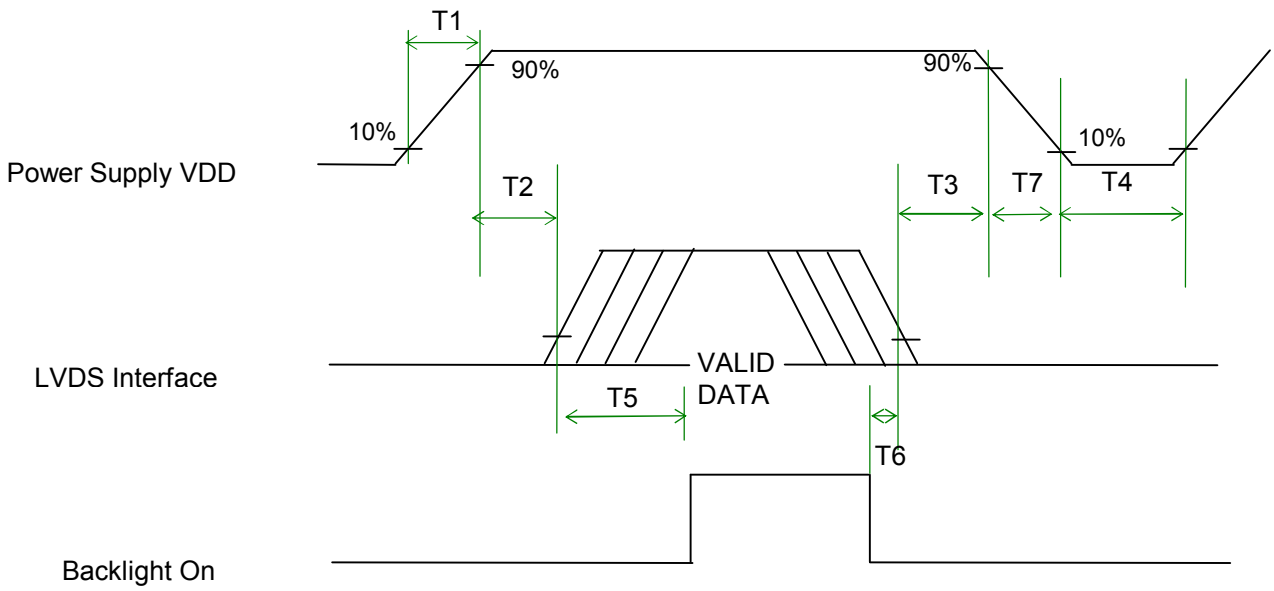
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

Test method:	Non-Operation
Acceleration:	1.5G
Frequency:	26 – 500Hz Random
Sweep:	30 Minutes each Axis (X,Y,Z)

8.2 Shock Test Spec:

Test Spec:

Test method:	Non-Operation
Acceleration:	260 G . Half sine wave
Active time:	2 ms
Pulse:	X,Y,Z .one time for each side

9. Reliability

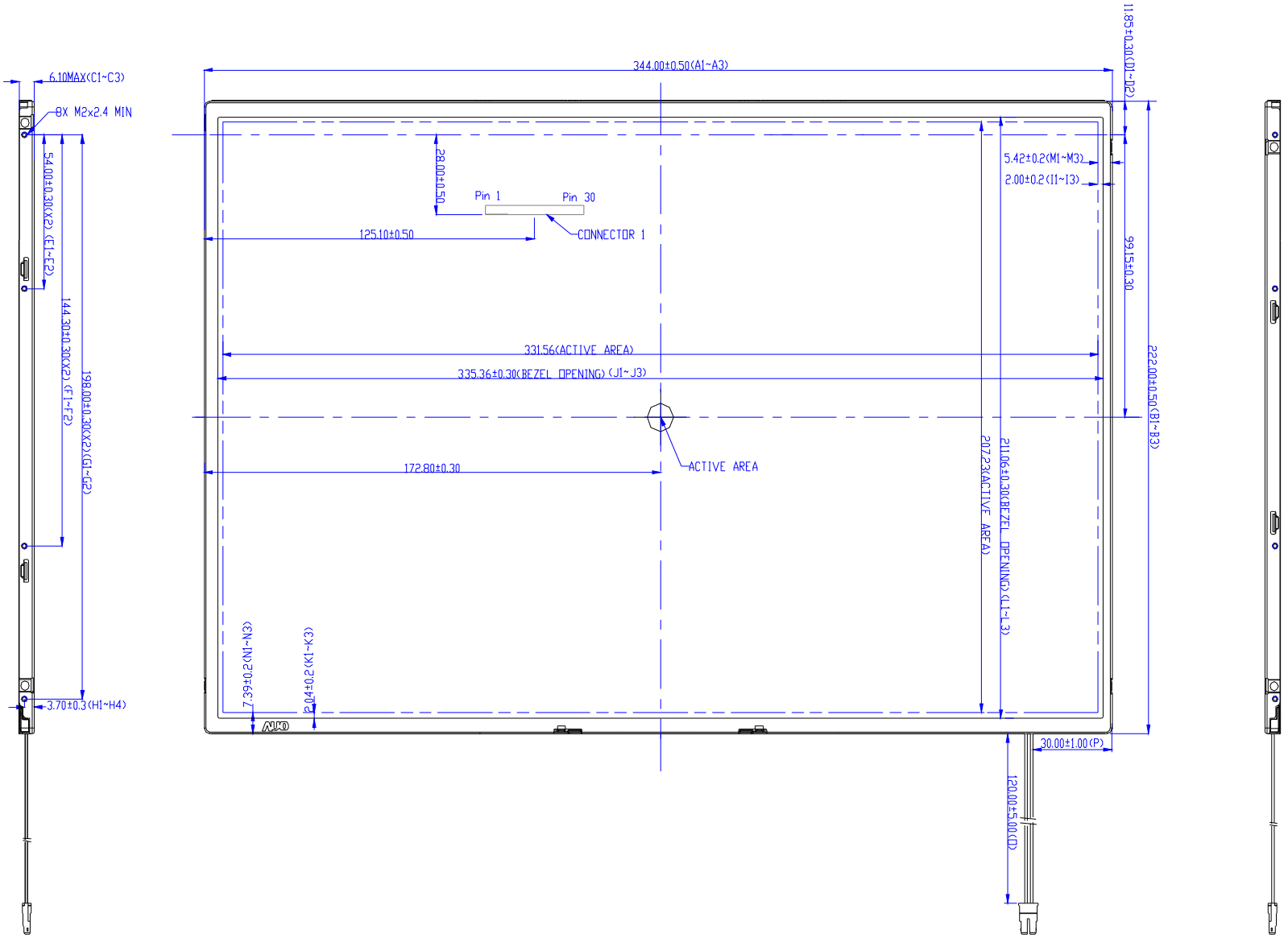
Items	Required Condition	Note
Temperature Humidity Bias	40℃/90%,300Hr	
High Temperature Operation	50℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hrs	
On/Off Test	25℃,150hrs(ON/30 sec. OFF/30sec., 10,000 cycles)	
Hot Storage	65℃/20% RH ,300 hours	
Cold Storage	-25℃/50% RH ,300 hours	
Thermal Shock Test	-25℃/30 min ,65℃/30 min 100cycles non-OP	
Shock Test (Non-Operating)	260G, 2ms, Half-sine wave, +/- X,Y,Z direction, 1 cycle	
Vibration Test (Non-Operating)	Sinusoidal vibration, 3.0 G zero-to-peak, 10 to 150 Hz, 30 mins in each of three mutually perpendicular axes	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Image sticking	10X10 checker pattern, 10 hrs, 25℃. The persisting pattern should be disappeared in 5 minutes	

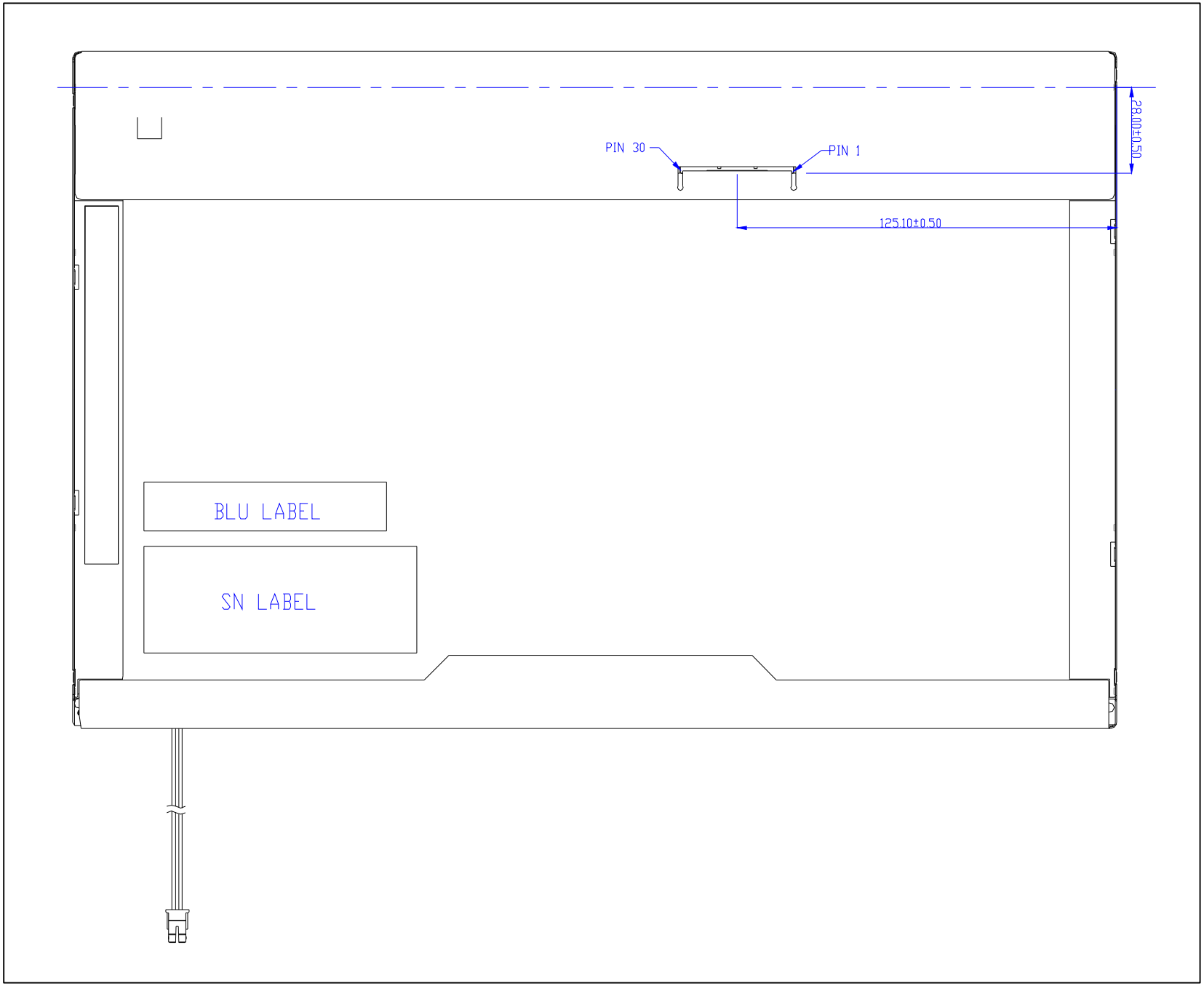
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

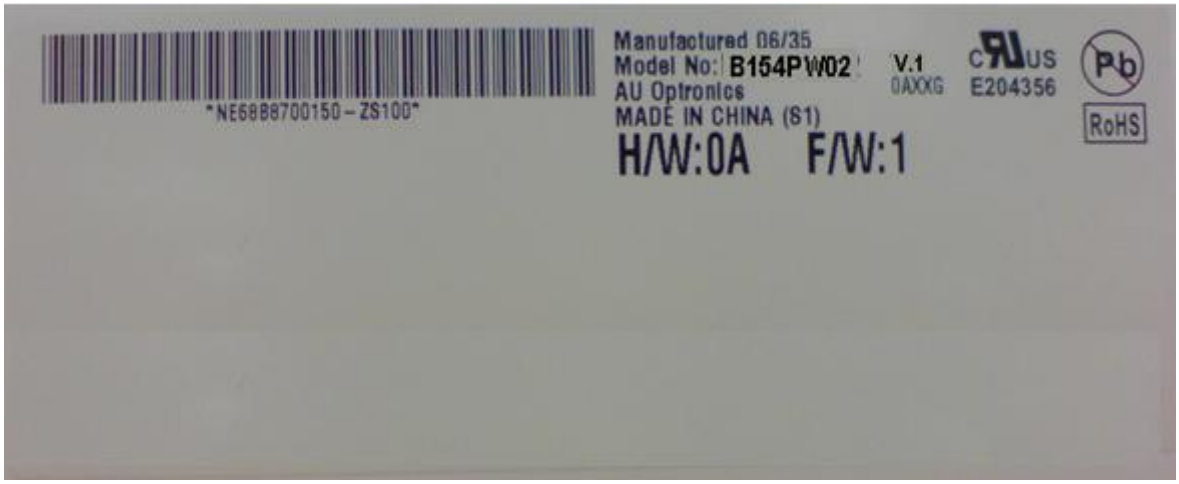
10. Mechanical Characteristics

10.1 LCM Outline Dimension

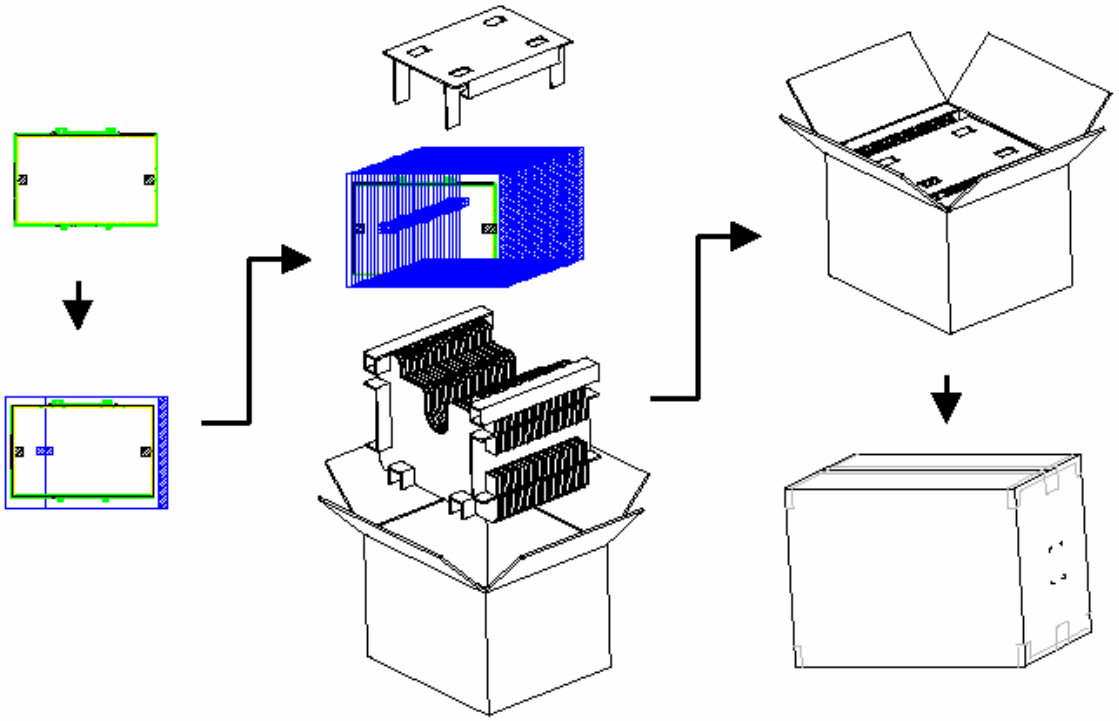



PIN 30
PIN 1
28.00±0.50
125.10±0.50
BLU LABEL
SN LABEL

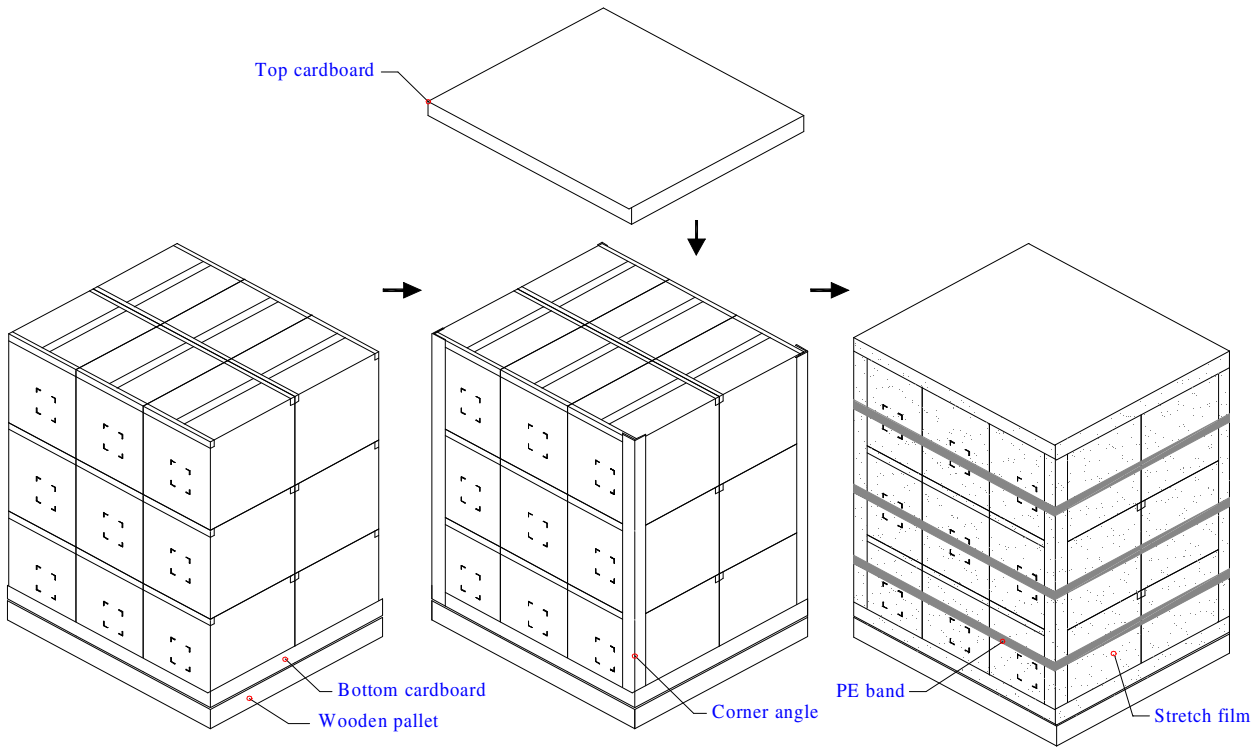
11.1 Shipping Label Format



11.2. Carton package



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

Address	FUNCTION	Value
HEX		HEX
00	Header	00
01		FF
02		FF
03		FF
04		FF
05		FF
06		FF
07		00
08	EISA Manuf. Code LSB	06
09	Compressed ASCII	AF
0A	Product Code	77
0B	hex, LSB first	21
0C	32-bit ser #	00
0D		00
0E		00
0F		00
10	Week of manufacture	01
11	Year of manufacture	10
12	EDID Structure Ver.	01
13	EDID revision #	03
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	80
15	**Max H image size** *(rounded to cm)*	21
16	**Max V image size** *(rounded to cm)*	15
17	**Display Gamma** *(=(gamma*100)-100)*	78
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A
19	Red/green low bits **(Lower 2:2:2:2 bits)**	1C
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5
1B	Red x **(Upper 8 bits)**	97
1C	Red y/ highER 8 bits	58
1D	Green x	50
1E	Green y	8E
1F	Blue x	27
20	Blue y	27
21	White x	50
22	White y	54
23	Established timing 1	00
24	Established timing 2	00
25	Established timing 3	00
26	Standard timing #1	01
27		01
28	Standard timing #2	01
29		01
2A	Standard timing #3	01
2B		01

2C	Standard timing #4	01
2D		01
2E	Standard timing #5	01
2F		01
30	Standard timing #6	01
31		01
32	Standard timing #7	01
33		01
34	Standard timing #8	01
35		01
36	Pixel Clock/10000 LSB	**9E**
37	Pixel Clock/10000 USB	**25**
38	Horz active **Lower 8bits**	A0
39	Horz blanking **Lower 8bits**	40
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	51
3B	Vertical Active **Lower 8bits**	84
3C	Vertical Blanking **Lower 8bits**	0C
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30
3E	HorzSync. Offset	40
3F	HorzSync.Width	20
40	VertSync.Offset : VertSync.Width	33
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00
42	Horizontal Image Size **Lower 8bits**	4B
43	Vertical Image Size **Lower 8bits**	CF
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10
45	Horizontal Border *(zero for internal LCD)*	00
46	Vertical Border *(zero for internal LCD)*	00
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18
48	Detailed timing/monitor	00
49	descriptor #2	00
4A		00
4B		0F
4C		00
4D		00
4E		00
4F		00
50		00
51		00
52		00
53		00
54		00
55		00
56		00
57		00
58		00
59		20
5A	Detailed timing/monitor	00
5B	descriptor #3	00
5C		00

5D		FE
5E		00
5F	Manufacture	41
60	Manufacture	55
61	Manufacture	4F
62		0A
63		20
64		20
65		20
66		20
67		20
68		20
69		20
6A		20
6B		20
6C	Detailed timing/monitor	00
6D	descriptor #4	00
6E		00
6F		FE
70		00
71	Manufacture P/N	42
72	Manufacture P/N	31
73	Manufacture P/N	35
74	Manufacture P/N	34
75	Manufacture P/N	50
76	Manufacture P/N	57
77	Manufacture P/N	30
78	Manufacture P/N	32
79	Manufacture P/N	20
7A	Manufacture P/N	56
7B	Manufacture P/N	31
7C		20
7D		0A
7E	Extension Flag	00
7F	Checksum	**13**