Doc. Version	3.0
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Product Specification

7.0" COLOR TFT-LCD MODULE

MODEL NAME: C070VW02 V0

RoHS Compliance

<◆>Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change

Record of Revision

Version	Revise Date	Page	Description
0.0	8.Dec,2005	--	Draft specification
0.1	21.Apr,2006	5	General Description – added backlight unit specification
		6	2.1.1 – Updated connector type
		8	2.2 – Modified VCOM
		8	3.1 – Modified AVDD
		8	3.1 – Modified VCOM
		9	3.3 & 3.4 – Modified AVDD condition
		12	5 – Modified response time Tr=6ms, Tf=10ms
		12	5 – Updated viewing angle
		15	7 – Updated front view outline dimension
		16	7 – Updated rear view outline dimension
		17	8 – Updated pcaking Form
		18	9.1 – Added gamma circuit
		19	9.2 – Modified power on/off sequence
0.2	12.May 2006	8	Updated V1~V5 MAX=
		16	6 – Update Outline Dimension – Front View
0.3	26.May 2006	15	Updated the vibration test conditions
0.4	13.Jul 2006	8	Updatd backlight connector type
		12	Updated pin description of connector
1.0	26.Sep 2006	13	Defined white chromaticity
1.1	13 Oct 2006	6	Modified connector type
2.0	8 Mar 2007	17	Updated mechanical drawing (alignment)
3.0	20 May 2008	6 ~ 9	Modified Pin Definition, function description, and note.
		11	Modified AC Timing Condition
		12 ~15	Modified Timing Diagrams
		23	Modified Power On/Off Sequence

Contents

General Description

The AUO Color amorphous silicon Thin Film Transistor LCD module is an active matrix Liquid Crystal Display produced by making the most of AUO's expertise in Flat Panel Display technologies having a 16:9 aspect ratio whose main application is navigation of automotive field.

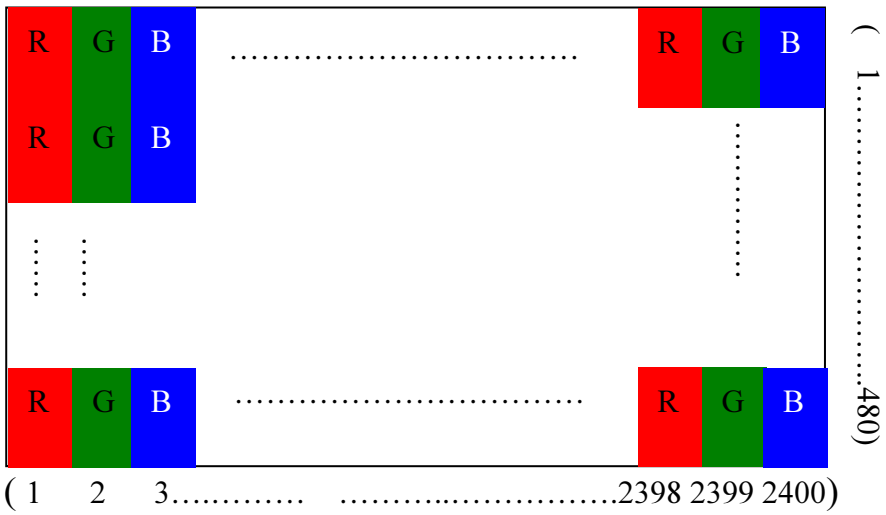
Features

- 15:9 aspect ratio suitable in wide-screen systems
- Higher resolution image composed of 384,000 pixel elements
- Wide viewing angle technology
- High contrast by Super Wide View technology
- Robust module design by using COG mounting technology
- Wide range of options input format by PCB design
- TN-normally white mode
- High power LEDs backlight with Mercury-free solution

1. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800RGB(H)×480(V)	
2	Active Area	mm	152.40(H)×91.44(V)	
3	Screen Size	inch	7.0(Diagonal)	
4	Pixel Pitch	mm	0.0635xRGB(H)×0.1905(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	Note 2
7	Overall Dimension	mm	165.0(H) × 104.0(V) × 5.5/9.15(T)	Note 3
8	Weight	g	150	
9	Panel surface treatment	--	AG(5% haze)	
10	Display Mode	--	Normally White	
11	Backlight Unit	--	High Power LEDs	

Note 1: Below figure shows the dot stripe arrangement.



Note 2: The 262K color display depends on 6-bit data signal input.

Note 3: The thickness is 5.5mm at the thin side and 9.15mm at the thick side (with PCB). Please refer to Sec 6, Outline Dimension for more details.

2. Electrical Specifications

2.1 Pin Assignment

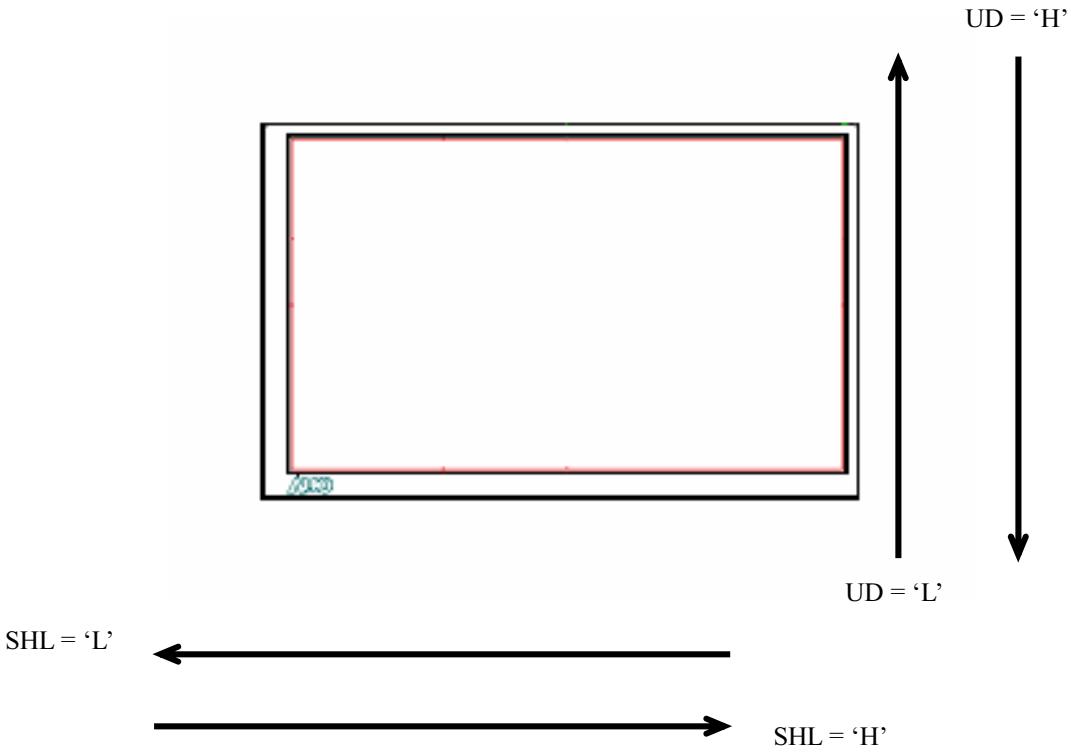
Connector type: PF050-O50B-C20 or compatible

Pin No	Symbol	I/O	Function	Remark
1	GND	P	Digital Ground for gate drive	
2	VCC	P	Digital voltage for gate driver	
3	VGL	P	TFT low voltage	
4	VGH	P	TFT high voltage	
5	STVL	I/O	Start pulse signal input/output (Vertical)	Note 1
6	STVR	I/O	Start pulse signal input/output (Vertical)	Note 1
7	CKV	I	Shift clock input for gate driver	
8	U/D	I	Up or Down display control	Note 1
9	OEV	I	Output enable, active low. The gate driver outputs are disable when OEV = "H".	
10	VCOM	I	Common electrode driving signal	
11	DIO1	I/O	Start pulse signal input/output (Horizontal)	Note 1
12	AVDD	P	Analog voltage for source driver	
13	AGND	P	Analog ground for source driver	
14	GND	P	Digital ground for source driver	
15	VCC (DVDD)	P	Digital voltage for source driver	
16	EDGSL	I	Select raising edge or raising/falling edge When EDGSL = "0", Latching source data onto the line latches at the rising edge When EDGSL = "1", Latching source data onto the line latches at the rising edge and falling edge	
17	CLK	I	Sampling and shifting clock pulse for source driver	
18	SHL(R/L)	I	Right or Left display control	Note 1
19	R0	I	Red data (LSB)	
20	R1	I	Red data	
21	R2	I	Red data	
22	R3	I	Red data	
23	R4	I	Red data	

24	R5	I	Red data (MSB)	
25	G0	I	Green Data (LSB)	
26	G1	I	Green Data	
27	G2	I	Green Data	
28	G3	I	Green Data	
29	G4	I	Green Data	
30	G5	I	Green Data (MSB)	
31	V1	I	Gamma Correction Reference Voltage	
32	V2	I	Gamma Correction Reference Voltage	
33	V3	I	Gamma Correction Reference Voltage	
34	V4	I	Gamma Correction Reference Voltage	
35	V5	I	Gamma Correction Reference Voltage	
36	V6	I	Gamma Correction Reference Voltage	
37	V7	I	Gamma Correction Reference Voltage	
38	V8	I	Gamma Correction Reference Voltage	
39	V9	I	Gamma Correction Reference Voltage	
40	V10	I	Gamma Correction Reference Voltage	
41	B0	I	Blue Data (LSB)	
42	B1	I	Blue Data	
43	B2	I	Blue Data	
44	B3	I	Blue Data	
45	B4	I	Blue Data	
46	B5	I	Blue Data (MSB)	
47	LD (OEH)	I	Latch and switch data to output	Note 2
48	REV	I	Control Whether RGB data are inverted or not When “REV” = 1 these data will be inverted. Ex. “00” ,” 3F” , “07” ,” 38” , and so on	
49	POL	I	Polarity selection	Note 3
50	DIO2	I/O	Start pulse signal input/output (Horizontal)	Note 1

I: Input pin; O: Output pin; I/O : Input or Output pin; P: Power

Note 1.



U/D	STVL	STVR	Direction
H	Output	Input	U → D
L	Input	Output	D → U

SHL	DIO1	DIO2	Direction
H	Input	Output	L → R
L	Output	Input	R → L

Note 2. LD

Latches the polarity of outputs and switches the new data to outputs.

1. At the rising edge, latches the "POL" signal to control the polarity of the outputs.

2. The pin also controls the switch of the line registers that switches the new incoming data to outputs.

Note 3. POL

"POL" value is latched at the rising edge of "LD" to control the polarity of the even or odd outputs.

"POL=1" represents that even outputs are of positive polarity with a voltage range from V1 to V5, and odd outputs are of negative polarity with a voltage range from V6 to V10. On the other hand, if LD gets low level "POL", even outputs are of negative polarity and odd outputs are of positive.

POL=1: Even outputs range from V1 ~ V5, and Odd outputs range from V6 ~ V10

POL=0: Even outputs range from V6 ~ V10, and Odd outputs range from V1 ~ V5

2.2 Absolute Maximum Ratings

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	Vcc	-0.3		5	V
	AVDD	-0.5		12	V
	VGH	-0.3		18	V
	VGL	-15		0.3	V
	VGH-VGL			33	V
Input Signal Voltage	Vi	-0.3		Vcc+0.3	V
	Vref(V1~V5)	0.4AVDD		AVDD+0.3	V
	Vref(V6~V10)	-0.3		0.6AVDD	V
	VCOM	4.0		4.4	V
Operating Temperature	Topa	-30		85	℃
Storage Temperature	Tstg	-40		85	℃
LED	Vf	11.2	13.2	15.2	V
	If		150	200	mA

3. Electrical Characteristics

3.1 Typical Operating Condition

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
	AVDD	9.7	9.8	9.9	V
	VGH	14.0	15.0	16.0	V
	VCOM	4.0	4.2	4.4	V
	VGL	-6.5	-7	-7.5	V
Input Reference Voltage	V1~V5	0.4AVDD	—	AVDD-0.1	V
	V6~V10	0.1	—	0.6AVDD	V
Input H/L level Voltage	VIH	0.8VCC	—	VCC	V
	VIL	0	—	0.2VCC	V

Note: All values should be measured under the condition of GND=AGND=0V

3.2 Current Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current For Driver	IGH	VGH=15V		100	150	uA
	IGL	VGL=-7V		-100	-150	uA
	ICC	VCC=3.3V		3.5	5	mA
	IDD	AVDD=9.8V		20	30	mA

3.3 LED Backlight Driving Condition (Connector : JST-PHR-2)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage	Vf			13.2	15.2	V
Current	If			150	200	mA
LED life time		Note 2	10,000	--	--	Hrs

Note 1: Panel surface temperature should be kept less than content of section 2.2. “Absolute maximum ratings"

Note 2: The ”LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃, If=150mA

3.4 AC Timing Condition

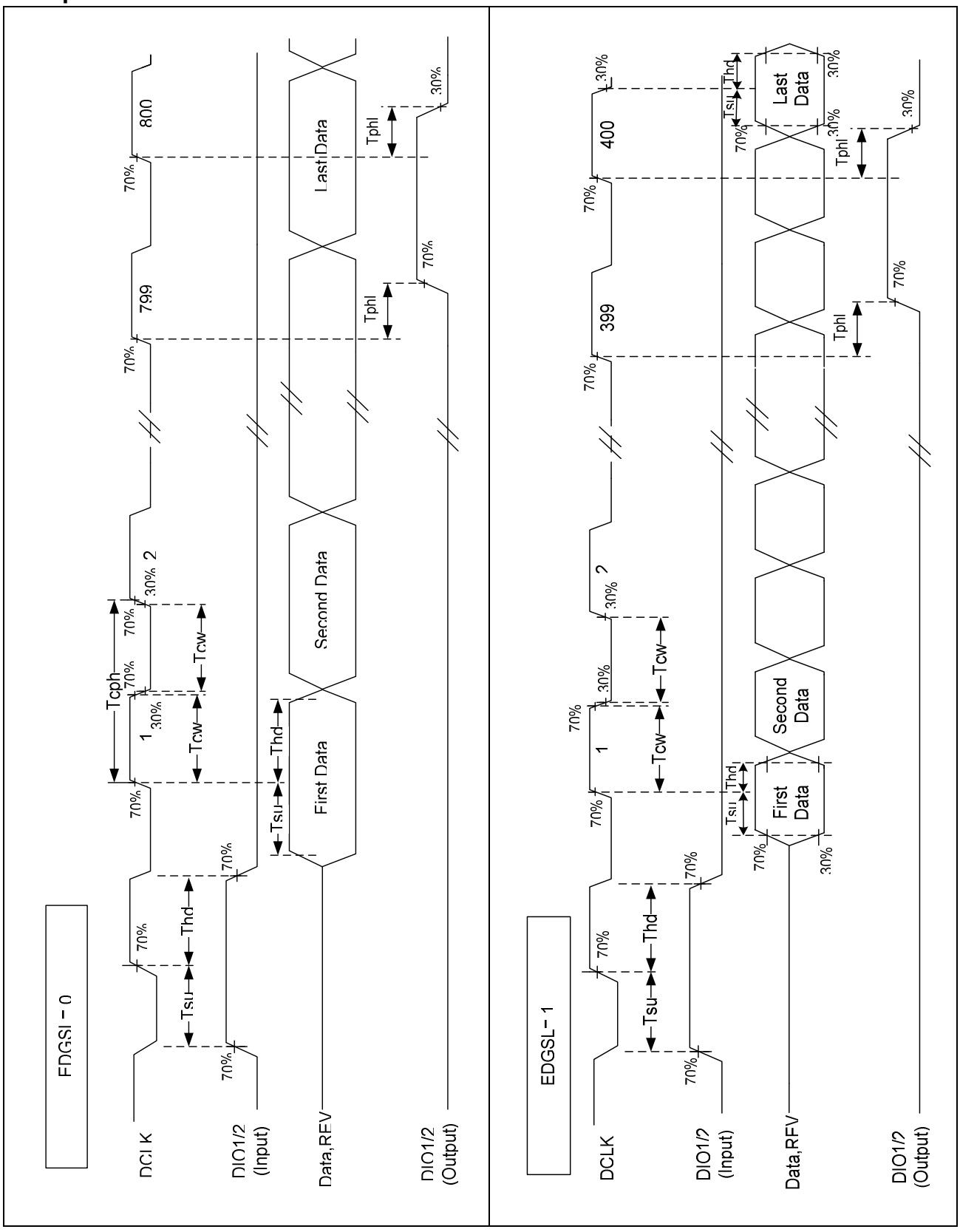
Characteristics (VCC=3.3V, AVDD=9.8V, AGND=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency (EDGSL = '0')	Fclk		33	44	MHz
DCLK frequency (EDGSL = '1')	Fclk		16.5	22	MHz
DCLK cycle time	Tcph	22.8	30		ns
DCLK pulse width	Tcw	40%		60%	Tcph
Data set-up time	Tsu	4			ns
Data hold time	Thd	2			ns
Propagation delay of DIO2/1	Tphl	6	10	15	ns
Time that the last data to LD	Tld	1			Tcph
Pulse width of LD	Twld	2			Tcph
Time that LD to DIO1/2	Tlds	5			Tcph
POL set-up time	Tpsu	6			ns
POL hold time	Tphd	6			ns
STV setup time	Tsuv	200			ns
STV hold time	Thdv	300			ns
CKV pulse width	Tckv	500			ns
Output stable time	Tst			15	us

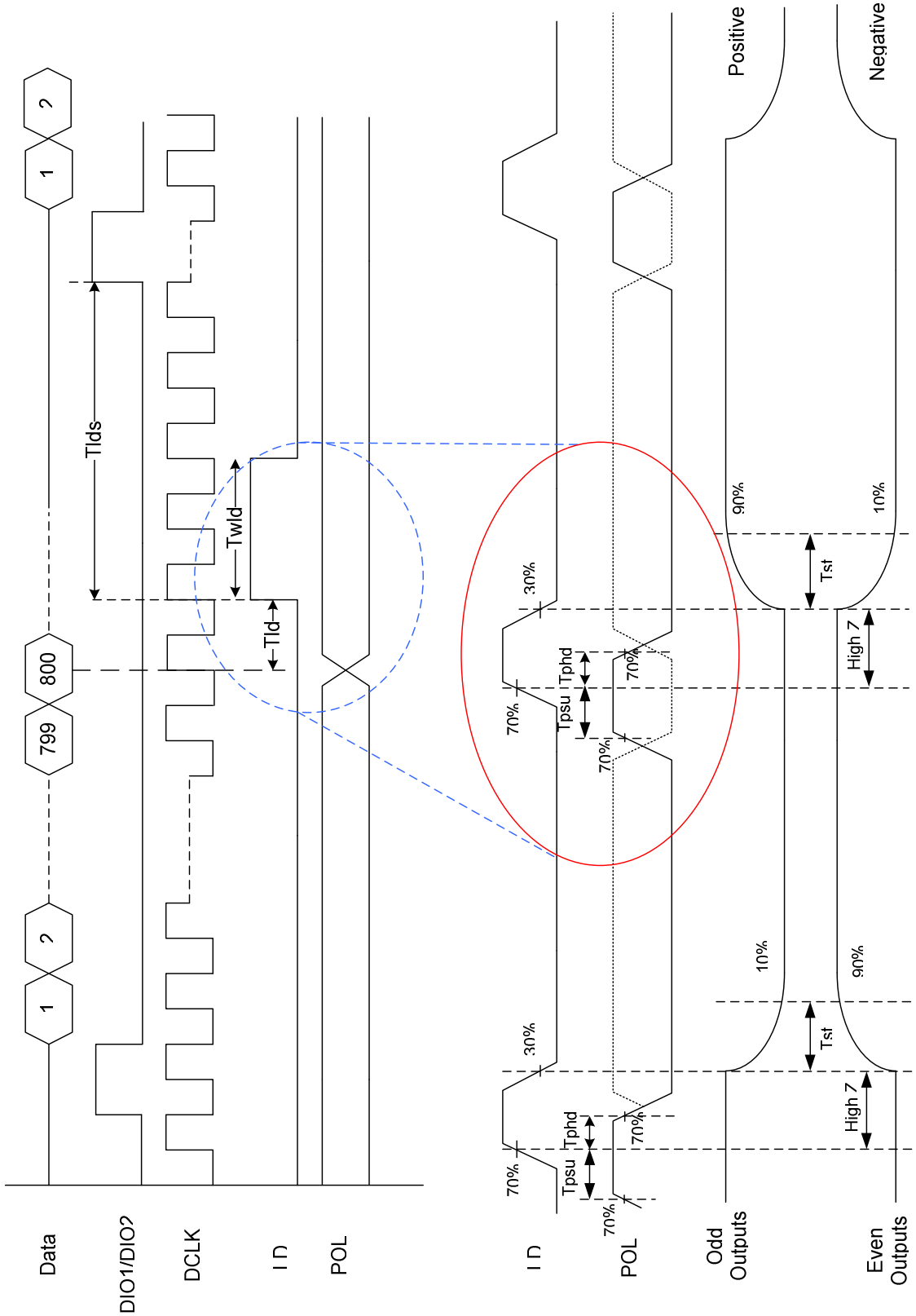
Note: The panel is designed to prevent the current leakage for the best display performance. If shorter discharge time is desired when system power off, then extra discharge circuit may be required at customer's side.

3.5 Timing Diagrams

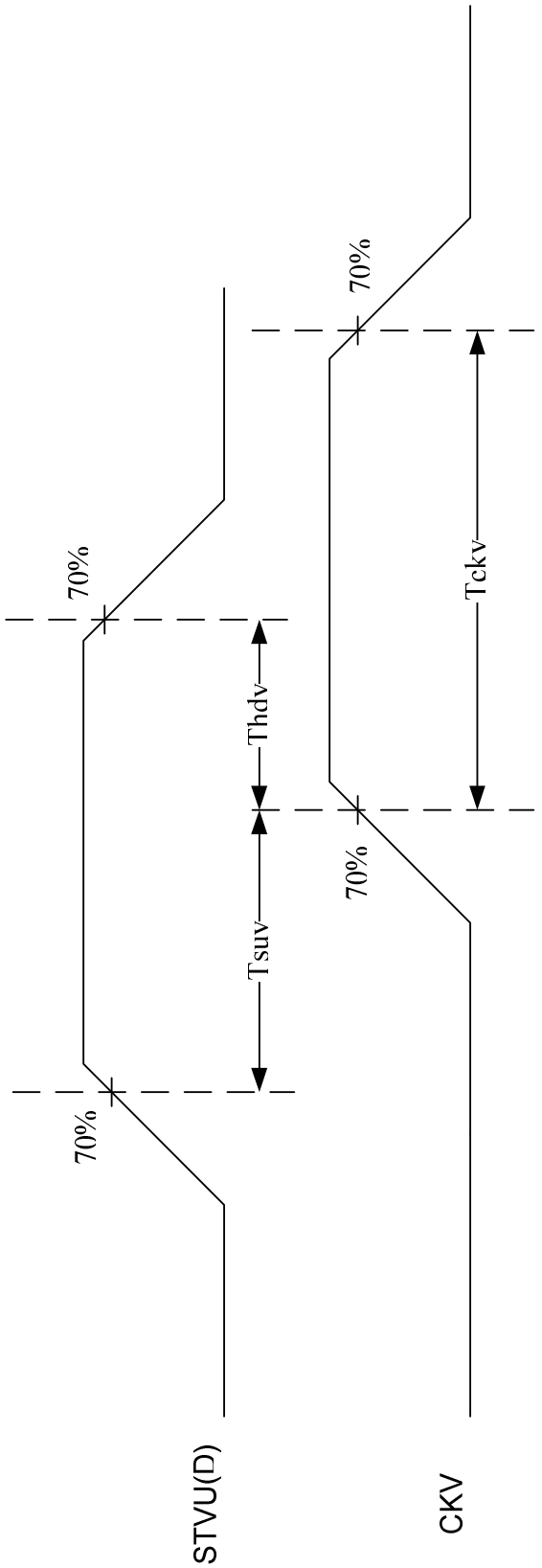
a. Operation Mode 1



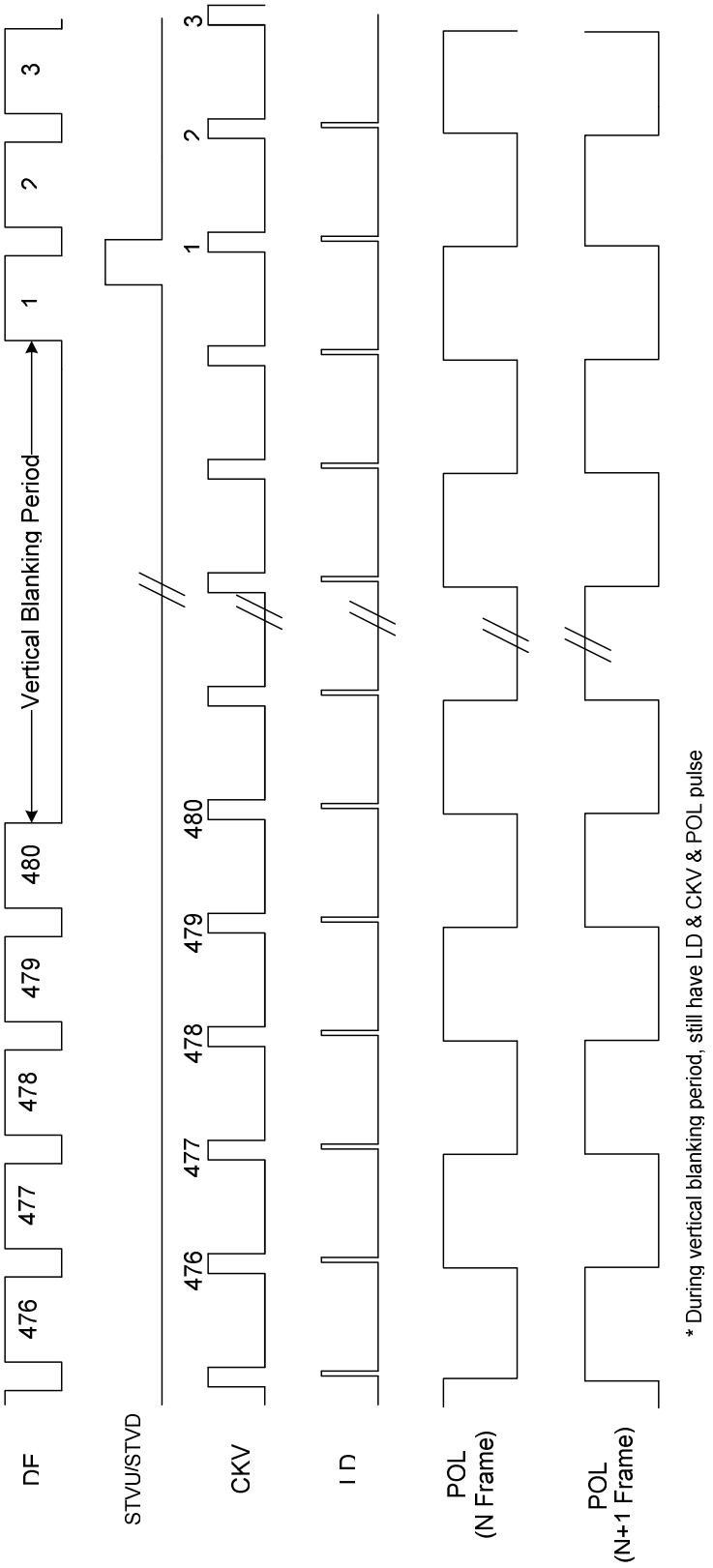
b. Horizontal timing



c. Vertical shift clock timing



d. Vertical timing (from up to down)



4. Optical Specifications

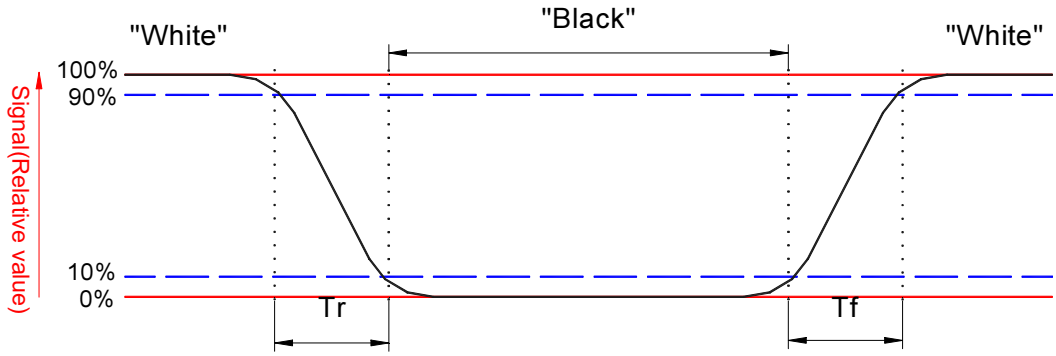
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ=0°	- -	6 10	10 20	ms ms	Note 3,5
Contrast ratio		CR	At optimized Viewing angle	200	300	-	-	Note 4, 5
Viewing angle	Top Bottom Left Right		CR≧10	30 50 50 50	40 60 60 60		deg.	Note 5
Viewing angle	Top Bottom Left Right		CR≧5	40 60 60 60	50 70 70 70		deg.	Note 5
Brightness		Y_L	If=150mA,25℃	300	400	-	nit	Note 6
White chromaticity		x	θ=0°	0.26	0.31	0.36		Note 6
		y	θ=0°	0.29	0.34	0.39		

Note 1 : Ambient temperature = 25℃, and lamp current If = 150 mA. To be measured in the dark room.

Note 2 :To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 3: Definition of response time:

The response time is defined as the time interval between the 10% and 90% of amplitudes. The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time).



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. White Vdata=V5 or V6

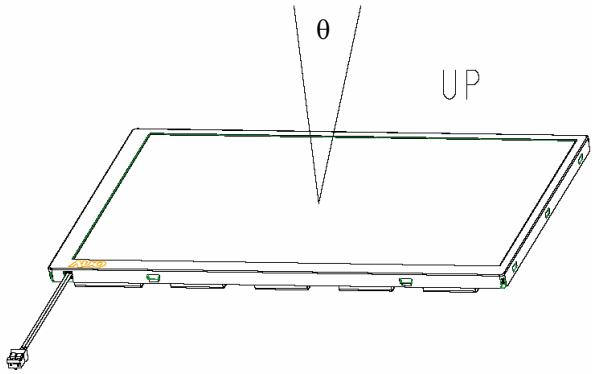
Black Vdata=V1 or V10

(For definition of V1, V5, V6 & V10, please refer to section 9.1)

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Brightness and White Chromaticity are measured at the center area of the panel at white frame.

Note 7. For definition of viewing angle please refer to figure as below.



5. Reliability Test Items

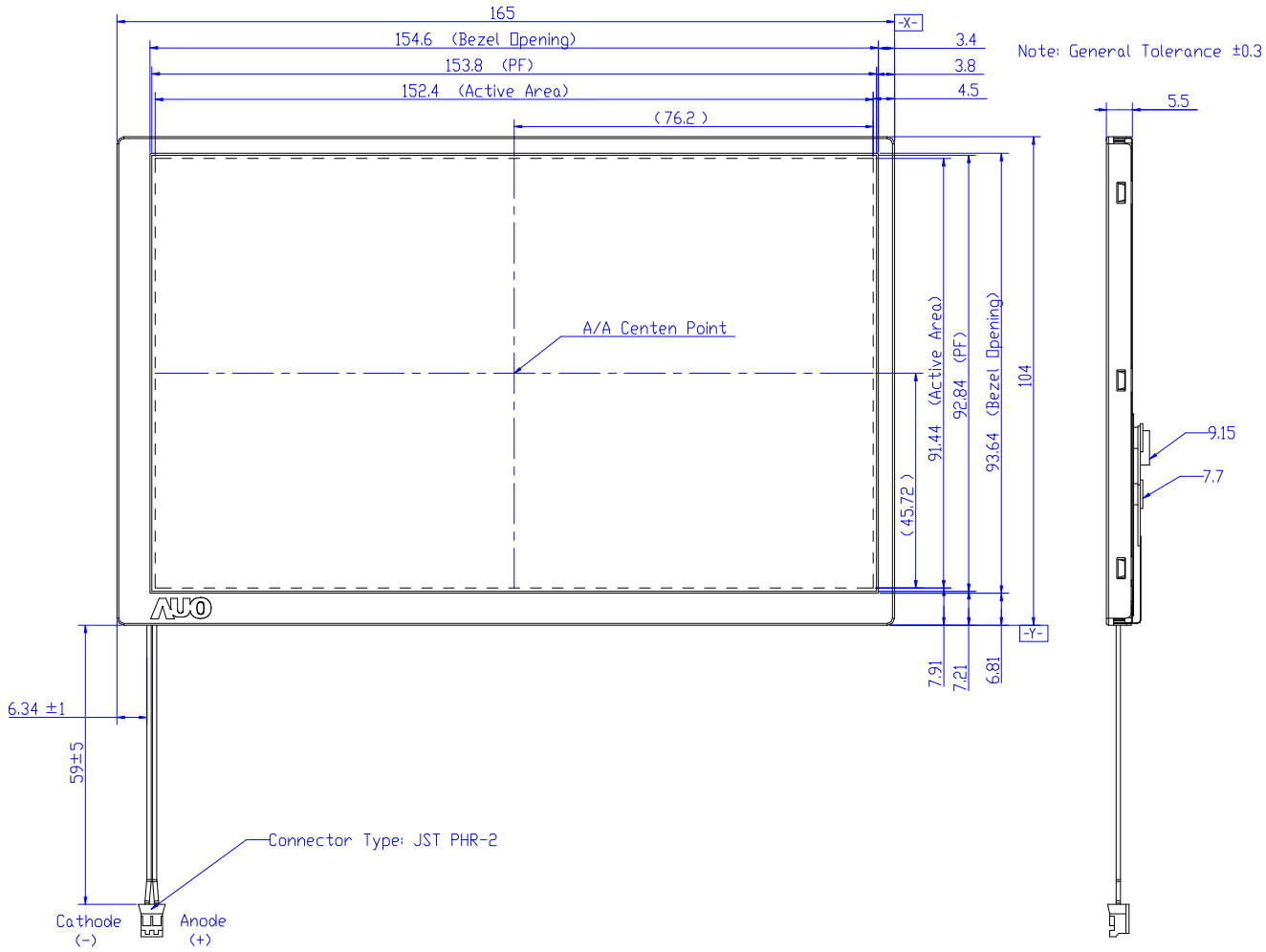
No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 85℃	240Hrs	
2	Low temperature storage	Ta= -40℃	240Hrs	
3	High temperature	Ta= 85℃	240Hrs	
4	Low temperature	Ta= -30℃	240Hrs	
5	High temperature and	Ta= 60℃, 90% RH	240Hrs	Operation
6	Heat shock	-30℃~85℃/100 cycles 1Hrs/cycle		Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal		Non-operation
8	Vibration	Frequency range	8~33.3Hz	JIS D1601,A10 Condition A
		Stoke	1.3mm	
		Sweep	2.9G, 33.3~400Hz	
		Cycle	15min.	
		2 hours for each direction of X, Z 4 hours for Y direction		
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction		
10	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

Note 1: Ta: Ambient temperature.

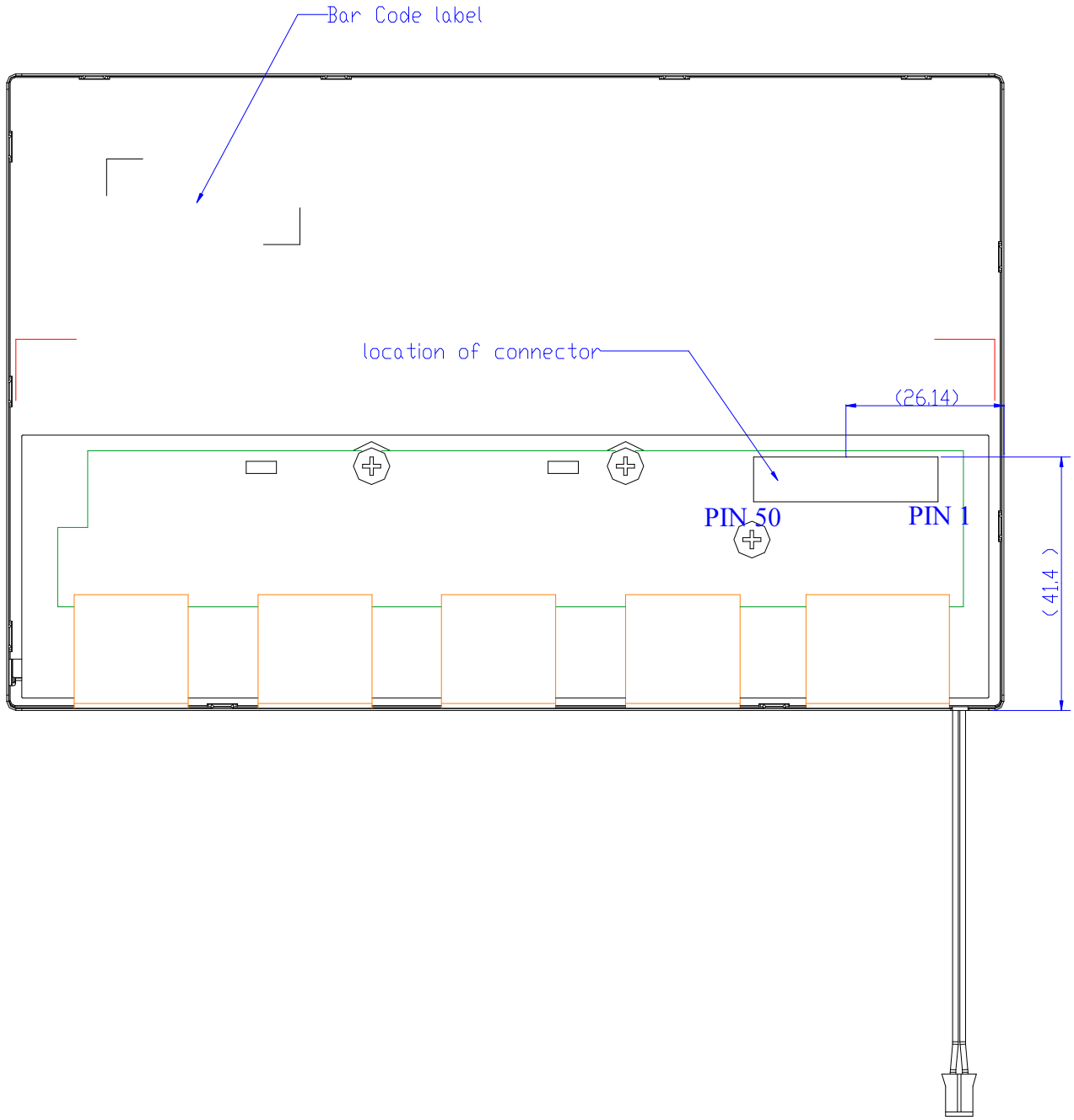
Note 2: In the standard conditions, there is not display function failure issue occurred. All the cosmetic specification is judged before the reliability stress.

6. Outline Dimension

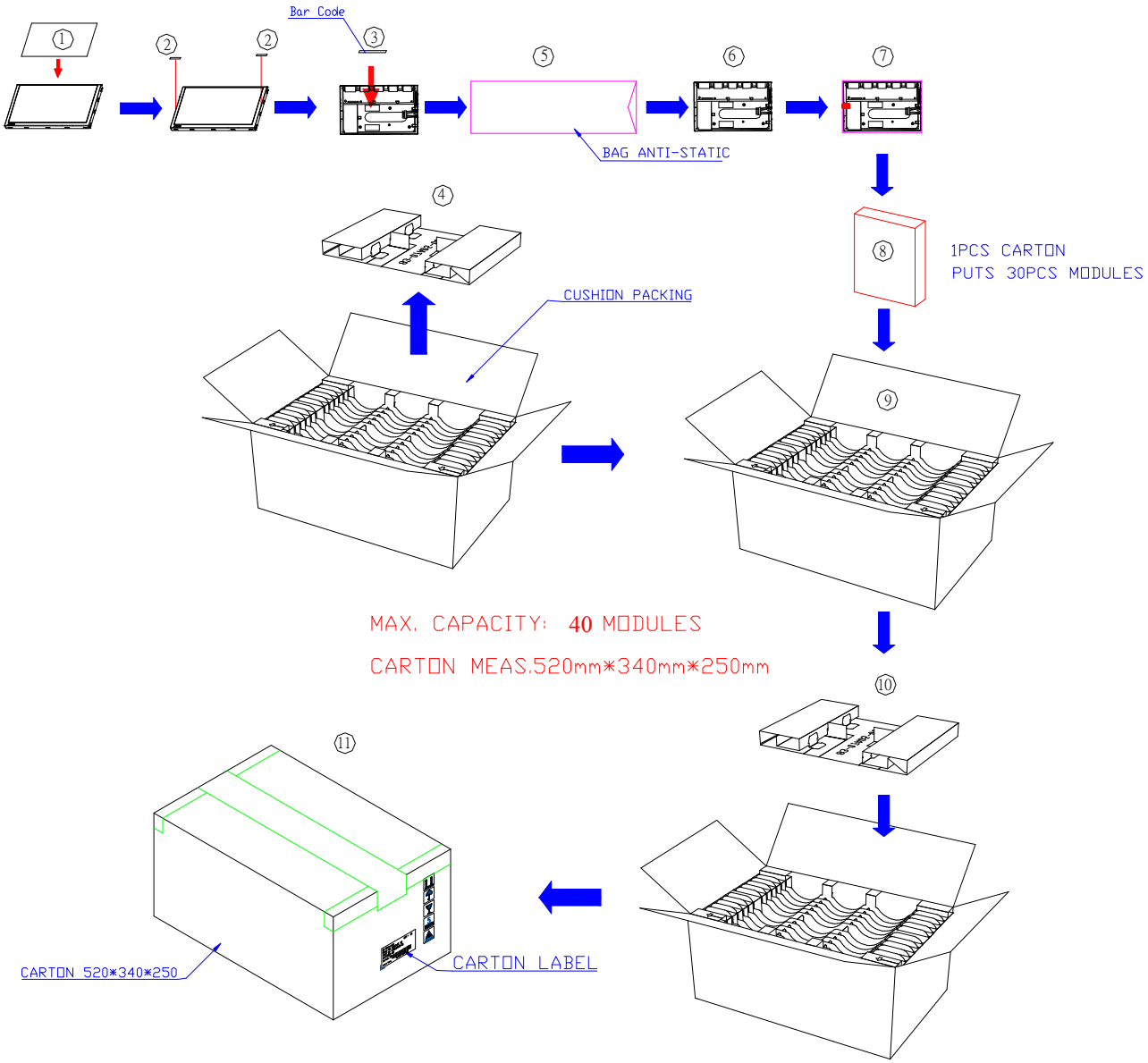
Front View



Rear View



7. Packing Form

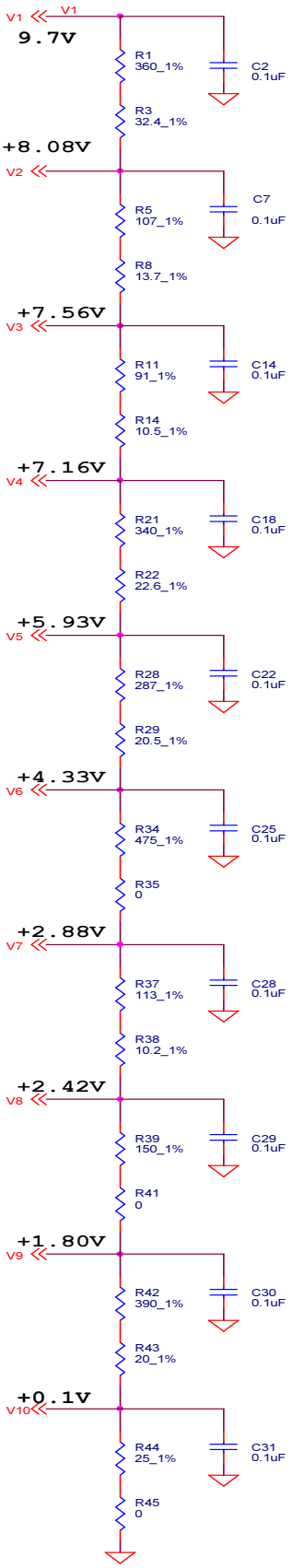


8. Application Notes

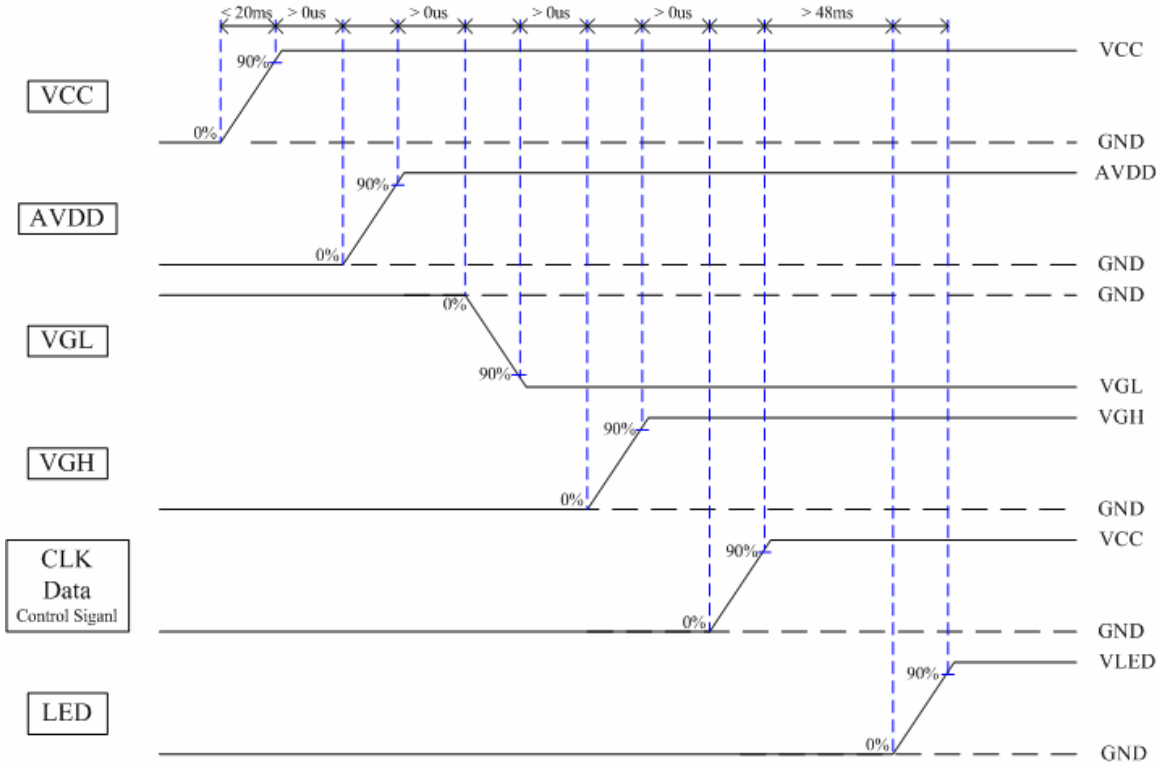
8.1 Typical application circuit

Gamma circuit:

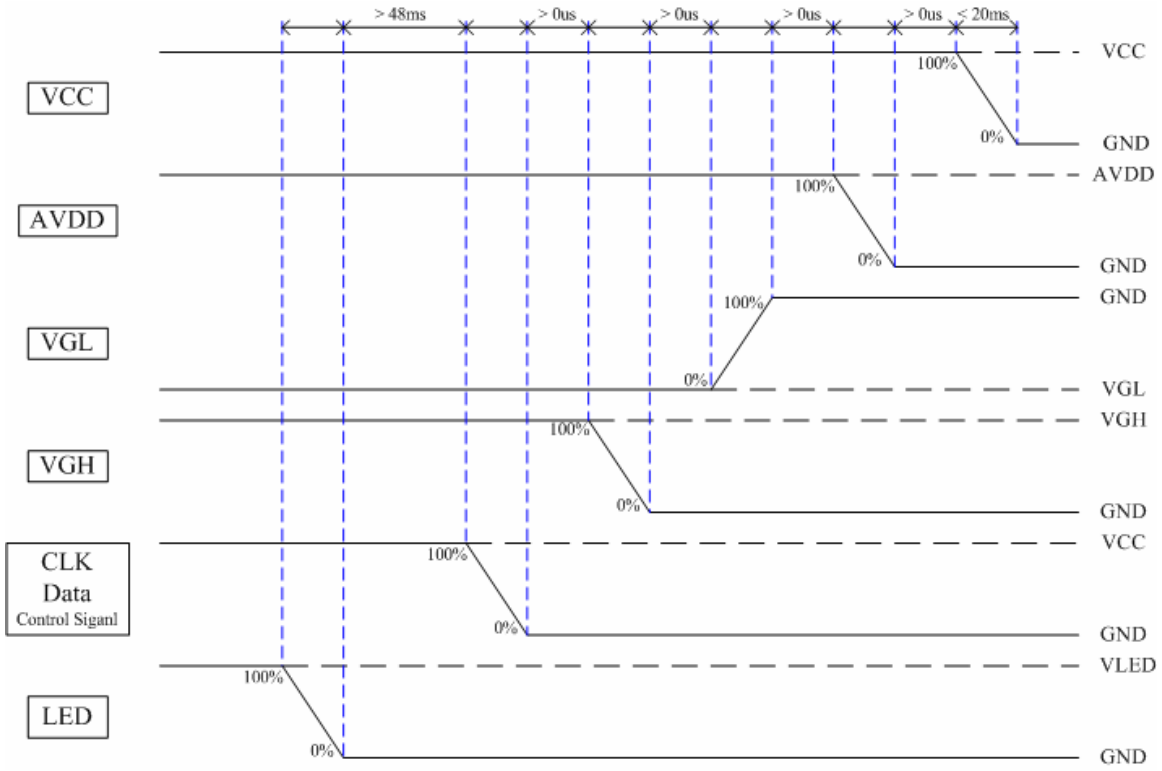
	AVDD	9.80
00H	V1	9.70
10H	V2	8.08
20H	V3	7.56
30H	V4	7.16
3FH	V5	5.93
3FH	V6	4.33
30H	V7	2.88
20H	V8	2.42
10H	V9	1.80
00H	V10	0.10



8.2 Power On/Off sequence



Power On Sequence



Power Off Sequence