HITACHI

Hitachi Displays, Ltd.

Tentative

Date : Oct. 13, 2004

TECHNICAL DATA
TX80D16VC0CAC

CONTENTS

RECORD OF REVISION

Date	The upper section : Before revision The lower section : After revision Sheet No.	Page	Summary

DESCRIPTION

The following specifications are applied to the following Super-TFT module.
Note : Inverter for back light unit is built in this module.

Product Name : TX80D16VC0CAC

General Specifications

Effective Display Area	: (H)697.6845×(V)392.256	(mm)
Number of Pixels	: (H)1,366×(V)768	(pixels)
Pixel Pitch	: (H)0.51075×(V)0.51075	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti-Glare	
Number of Colors	: 16,777,216	(colors)
Viewing Angle Range	: Super Wide Version (Horizontal & Vertical : 170°, CR≧10)	
Input Signal	: 1-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 16 pcs. of CCFL	
External Dimensions	: (H)780.0×(V)450.0×(t)50.5	(mm)
Weight	: 8,500g typ.	

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1),5)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	14.7 (1.5G)	m/s 2	3)
Shock	-	29.4(3G)	-	294 (30G)	m/s 2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 70℃ on the condition of operating.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) Ta≦40 ℃·····Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta＞ 40 ℃·····Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.
All mounting holes should be fixed. (Side mounting hole (4 locations), Top mounting hole (4 locations), Rear mounting hole (4 locations)).

5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
However, it does not affect the characteristics and reliability of the product.

1.2 Electrical Absolute Maximum Ratings

(1)Super-TFT Module

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	13.2	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient ：200pF-250Ω, Environmental ：25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light Inverter

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Voltage	Vin	0	32	V	
ON/OFF Control Input Voltage	ON/OFF	0	5.5	V	
Brightness Control Input Voltage	BRT	0	5.5	V	

2. OPTICAL CHARACTERISTICS

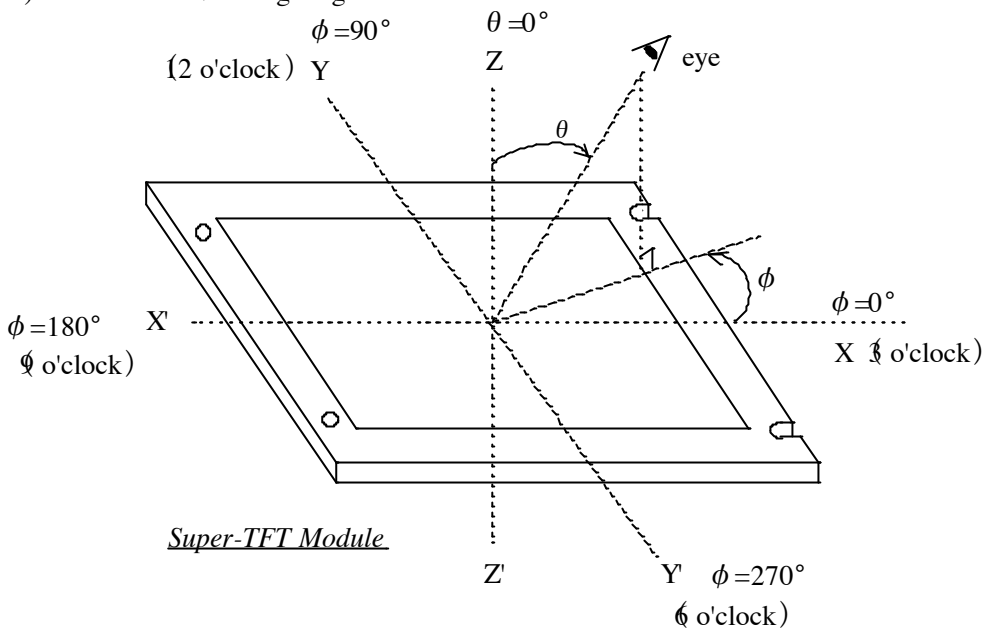
The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

Measuring equipment :Pritchard 1980A, or equivalent

Temperature =25°C、VDD=12.0V、f V=60Hz、BRT:High(Duty:100%)

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR		500	800	—	-	2)
Response Time	Rise	ton		-	10	20	ms	3)
	Fall	toff		-	9	20	ms	3)
Brightness of white		Bwh		400	500	—	cd/m 2	
Brightness uniformity		Buni		-	-	25	%	4)
Color Chromaticity (CIE)	Red	χ	θ =0° 1)	0.61	0.64	0.67	-	[Gray scale =255]
		y		0.29	0.32	0.35		
	Green	χ		0.26	0.29	0.32		
		y		0.58	0.61	0.64		
	Blue	χ		0.12	0.15	0.18		
		y		0.04	0.07	0.10		
	White	χ		0.251	0.281	0.311		
		y		0.258	0.288	0.318		
Variation of Color Position (CIE)	Red	Δ χ	θ =+50° φ =0°,90° 180°,270° 1)	-	-	0.04	-	5) [Gray scale =255]
		Δ y		-	-	0.04		
	Green	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
	Blue	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
	White	Δ χ		-	-	0.04		
		Δ y		-	-	0.04		
Contrast Ratio at 85°		CR85°		10	-	-	-	Estimated value

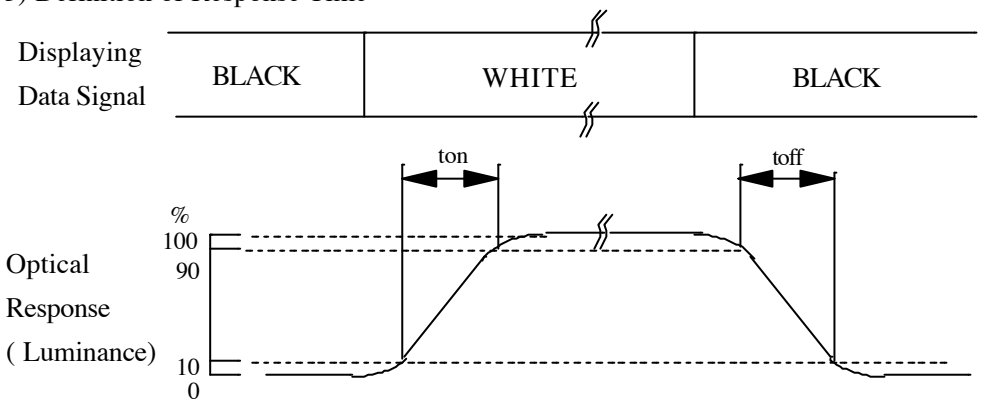
Note 1) Definition of Viewing Angle



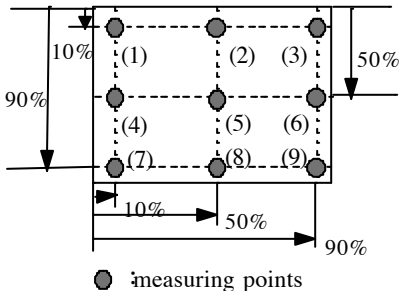
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level) . The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \frac{|\,Bmax \text{ or } Bmin - Bave\,|}{Bave} \times 100$$

where, Bmax = Maximum brightness

Bmin = Minimum brightness

$$Bave = \text{Average brightness} = \frac{\sum_{k=1}^{9} (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at $\theta = 0°$ and at $\theta = 50°$ & $\phi = 0°, 90°, 180°, 270°$.

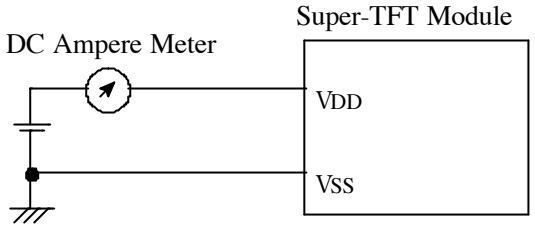
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD Module

Ta=25°C, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VDD	11.4	12.0	12.6	V	
Power Supply Current	IDD	-	0.5	0.8	A	1),2)
Ripple Voltage of Power Supply	VDDR	-	-	0.15	V	

Note 1) DC current at fv=60.0Hz, fCLK=85MHz, VDD=12.0V and Display pattern is white.



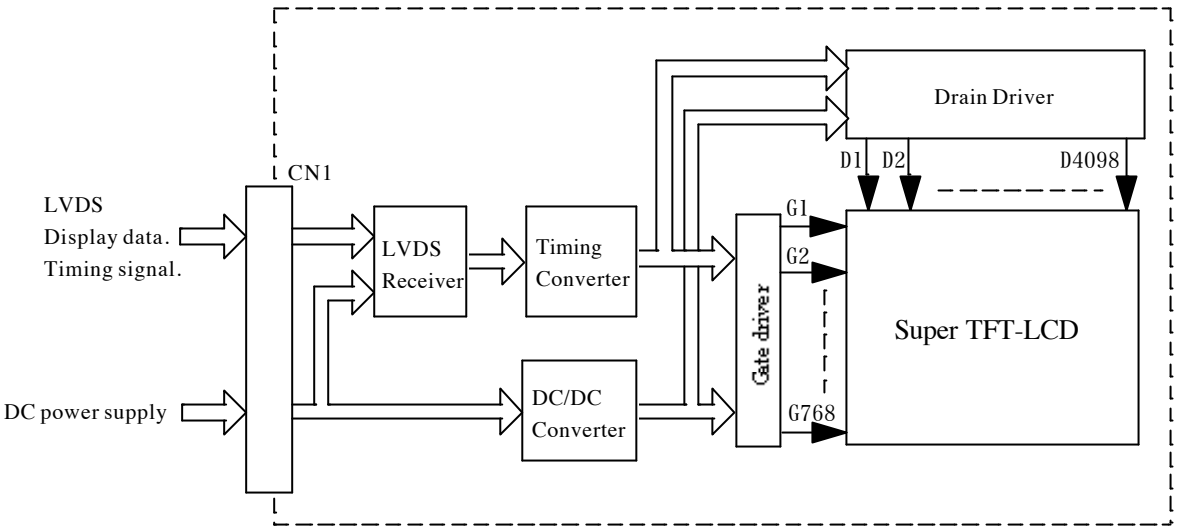
2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of power supply.

3.2 Back Light

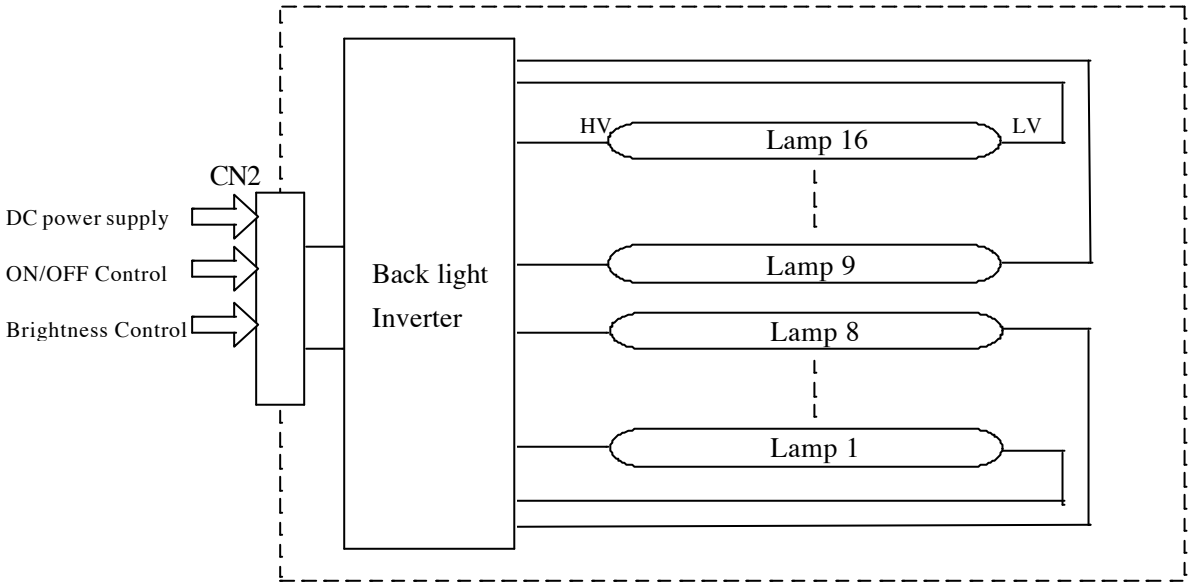
ITEM		Symbol	VALUE			Unit	Notes
			Min	Typ	Max		
Input Voltage		Vin	21.6	24.0	26.4	V	
Input Current		Iin	-	4.5	6.5	A	at Max Brightness. Vin=Min～Max
ON/OFF Control Input Voltage	ON	ON/OFF	2.2	-	5.5	V	
	OFF		0	-	0.8	V	
Brightness Control Input Voltage	Min.Brightness	BRT	-	0	-	V	
	Max.Brightness		3.0	-	3.3	V	
Output Current		IL	4.5	5.0	5.5	mArms	BRT=3.3V
PWM Duty	Min.Brightness	On-Duty	-	20	-	%	BRT=0V
	Max.Brightness		100	-	-		BRT=3.3V
Lamp Voltage		VL	-	(1200)	-	Vrms	Ta=25°C
Starting Voltage		Vs	1600	-	-	Vrms	Ta=0°C
Output Frequency		f	50	55	60	kHz	

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



5. INTERFACE PIN ASSIGNMENT

5. 1 TFT-LCD MODULE

CN1 : JAE FI-X30SSL-HF

(Matching connector : JAE FI-X30C2L or equivalent)

Pin No.	Symbol	Description	Note
1	VDD	Power Supply (typ.+12V)	1)
2	VDD		
3	VDD		
4	VDD		
5	VSS	GND(0V)	2)
6	VSS		
7	VSS		
8	VSS		
9	VSS		
10	VSS		
11	VSS		
12	Rx0-	Pixel Data	3)
13	Rx0+		
14	VSS	GND(0V)	2)
15	Rx1-	Pixel Data	3)
16	Rx1+		
17	VSS	GND(0V)	2)
18	Rx2-	Pixel Data	3)
19	Rx2+		
20	VSS	GND(0V)	2)
21	CLK-	Pixel Clock	3)
22	CLK+		
23	VSS	GND(0V)	2)
24	Rx3-	Pixel Data	3)
25	Rx3+		
26	VSS	GND(0V)	2)
27	NC		
28	NC		
29	VSS	GND(0V)	2)
30	VSS		

Notes 1) All VDD pins shall be connected to +12.0V(Typ.).

2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.

3) Rx n+ and Rx n- (n=1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

5. 2 BACK-LIGHT UNIT

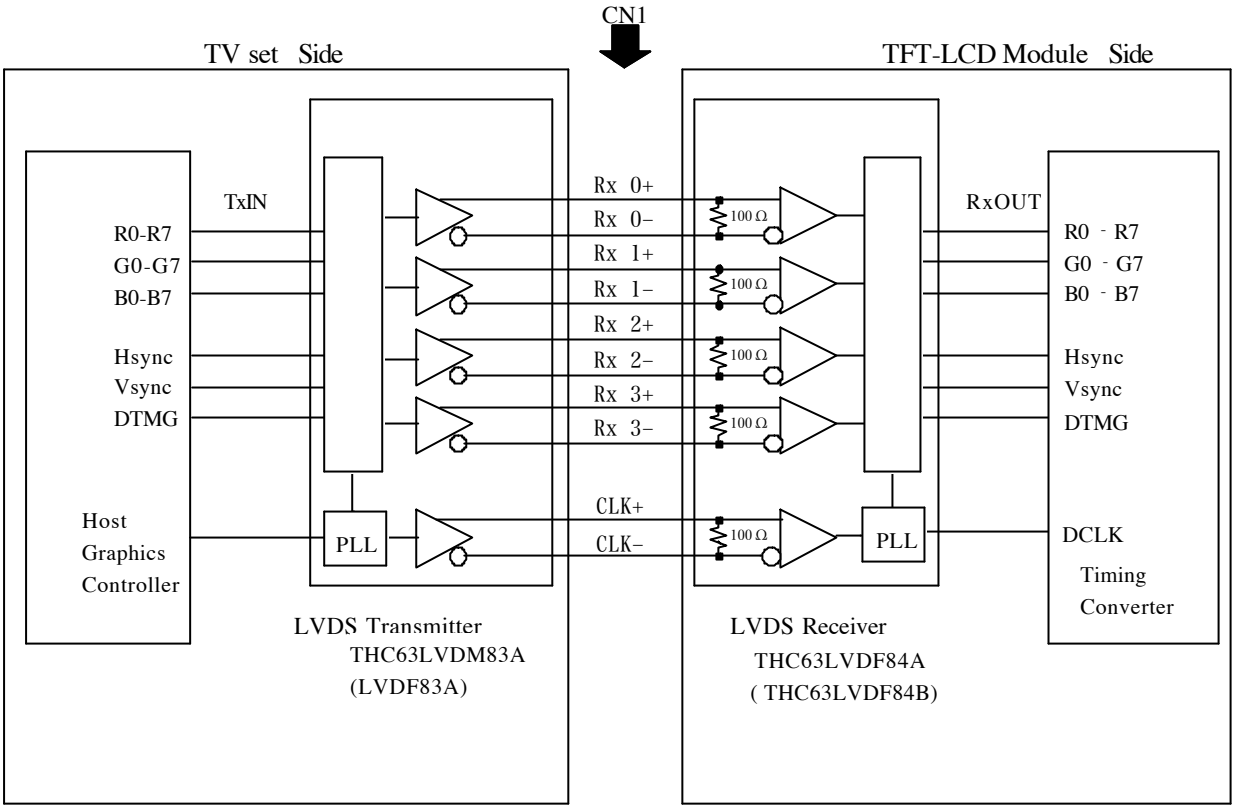
CN2 : JST S14B-PH-SM3-TB

(Matching connector : JST PHR-14 or equivalent)

Pin No.	SYMBOL	Description	Note
1	VIN	Power supply (Typ. 24V)	1)
2	VIN		
3	VIN		
4	VIN		
5	VIN		
6	VSS	GND (0V)	2)
7	VSS		
8	VSS		
9	VSS		
10	VSS		
11	NC		
12	ON/OFF	High:Lamp ON, Low:Lamp OFF	3)
13	BRT	High:Max.Brightness, Low:Min. Brightness	4)
14	VSS	GND (0V)	2)

Notes 1) All VIN pins shall be connected to +24.0V (Typ.).
2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.
3) High level:2.2～5.5V, Low level:0～0.8V
4) High level:3.0～3.3V, Low level:0V

BLOCK DIAGRAM OF INTERFACE



R0～R7	: Pixel R Data
G0～G7	: Pixel G Data
B0～B7	: Pixel B Data
HSYNC	: Horizontal synchronization signal
VSYNC	: Vertical synchronization signal
DTMG	: Display timing signal

Notes 1) The system must have the transmitter to drive the module.
2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

LVDS INTERFACE

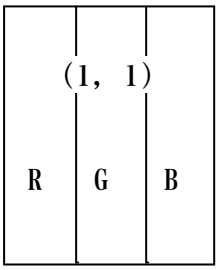
	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL
		PIN	INPUT	PC	TFT-LCD	PIN	OUTPUT	INPUT
24bit	R2	51	Tx IN0	TA OUT0+	Rx 0+	27	Rx OUT0	R2
	R3	52	Tx IN1			29	Rx OUT1	R3
	R4	54	Tx IN2			30	Rx OUT2	R4
	R5	55	Tx IN3			32	Rx OUT3	R5
	R6	56	Tx IN4			33	Rx OUT4	R6
	R7	3	Tx IN6	TA OUT0-	Rx 0-	35	Rx OUT6	R7
	G2	4	Tx IN7			37	Rx OUT7	G2
	G3	6	Tx IN8	TA OUT1+	Rx 1+	38	Rx OUT8	G3
	G4	7	Tx IN9			39	Rx OUT9	G4
	G5	11	Tx IN12			43	Rx OUT12	G5
	G6	12	Tx IN13			45	Rx OUT13	G6
	G7	14	Tx IN14	TA OUT1-	Rx 1-	46	Rx OUT14	G7
	B2	15	Tx IN15			47	Rx OUT15	B2
	B3	19	Tx IN18			51	Rx OUT18	B3
	B4	20	Tx IN19	TA OUT2+	Rx 2+	53	Rx OUT19	B4
	B5	22	Tx IN20			54	Rx OUT20	B5
	B6	23	Tx IN21			55	Rx OUT21	B6
	B7	24	Tx IN22			1	Rx OUT22	B7
	HSYNC	27	Tx IN24	TA OUT2-	Rx 2-	3	Rx OUT24	HSYNC
	VSYNC	28	Tx IN25			5	Rx OUT25	VSYNC
	DTMG	30	Tx IN26			6	Rx OUT26	DTMG
	R0	50	Tx IN27	TA OUT3+	Rx 3+	7	Rx OUT27	R0
	R1	2	Tx IN5			34	Rx OUT5	R1
	G0	8	Tx IN10			41	Rx OUT10	G0
	G1	10	Tx IN11			42	Rx OUT11	G1
	B0	16	Tx IN16	TA OUT3-	Rx 3-	49	Rx OUT16	B0
	B1	18	Tx IN17			50	Rx OUT17	B1
	RSVD 1)	25	Tx IN23			2	Rx OUT23	not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0～R7 : Pixel R Data (7 ; MSB, 0 ; LSB)
G0～G7 : Pixel G Data (7 ; MSB, 0 ; LSB)
B0～B7 : Pixel B Data (7 ; MSB, 0 ; LSB)
HSYNC : Horizontal synchronization signal
VSYNC : Vertical synchronization signal
DTMG : Display timing signal

Notes 1) RSVD(reserved) pins on the transmitter shall be "H" or "L".

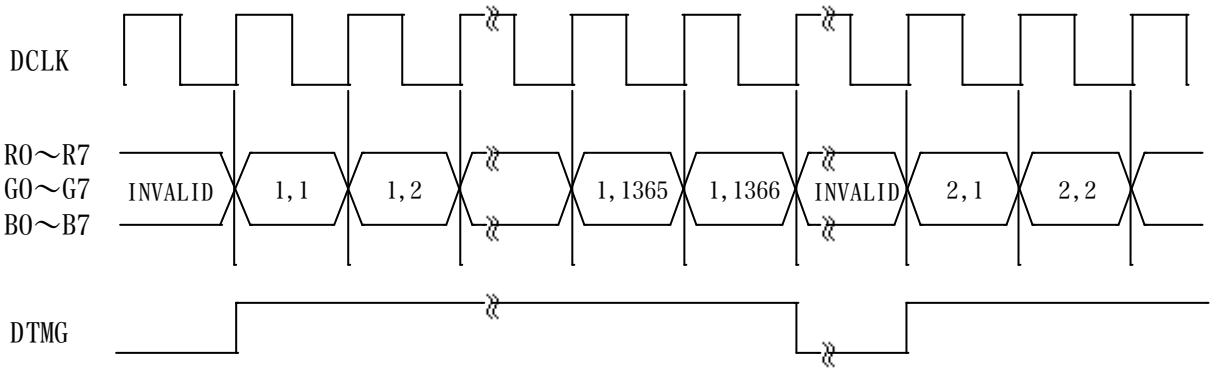
CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent one pixel is latched during one cycle of DCLK.



pixel : R0～R7 :R data
G0～G7 :G data
B0～B7 :B data

1,1	1,2	1,3	----------	1,1366
2,1	2,2	2,3	----------	2,1366
3,1	3,2	3,3	----------	3,1366
⋮	⋮	⋮		⋮
768,1	768,2	768,3	----------	768,1366



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color	Input	Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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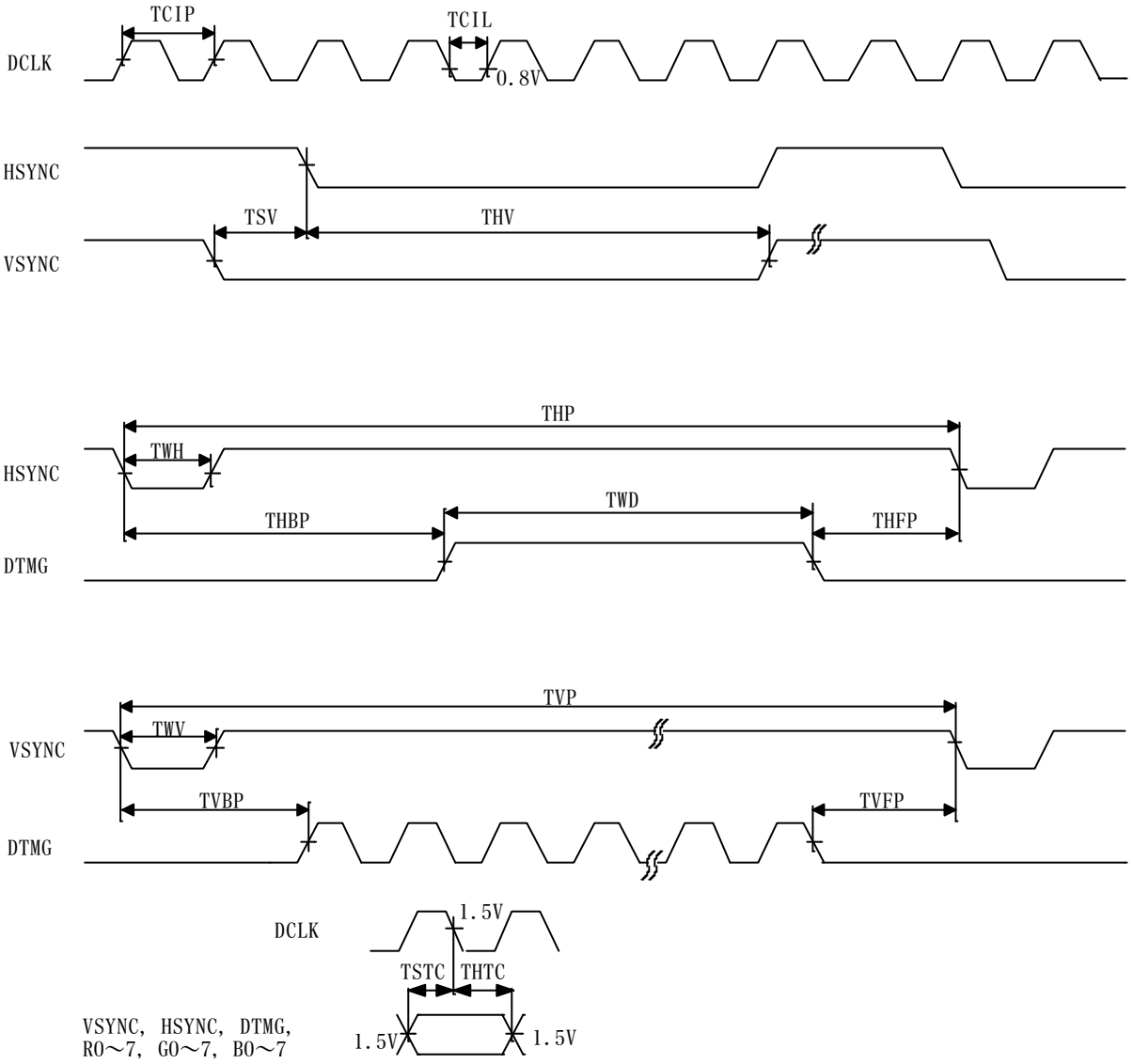
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes 1) Definition of gray scale:
Color(n)・・・・Number in parenthesis indicates gray scale level. Larger n corresponds to brighter level.

2) Data: 1:High, 0:Low

6. INTERFACE TIMING

6.1 TIMING CHART



Notes 1) Reference level for each timing signal is 1.5V unless it is stated on the chart , high level voltage(VIH) and low level voltage(VIL) are defined as follows:

$V_{IH} \geqq 2.0$ V $V_{IL} \leqq 0.8$ V

The above definition conforms to the specifications of LVDS transmitter (THC63LVDM83A / by THine Microsystems, Inc.).

2) The timing of DCLK to other signals conforms to the specifications of LVDS transmitter.

3) HSYNC, VSYNC timing is specified in negative polarity.

4) HSYNC pulse is needed while data is invalid (blanking period).

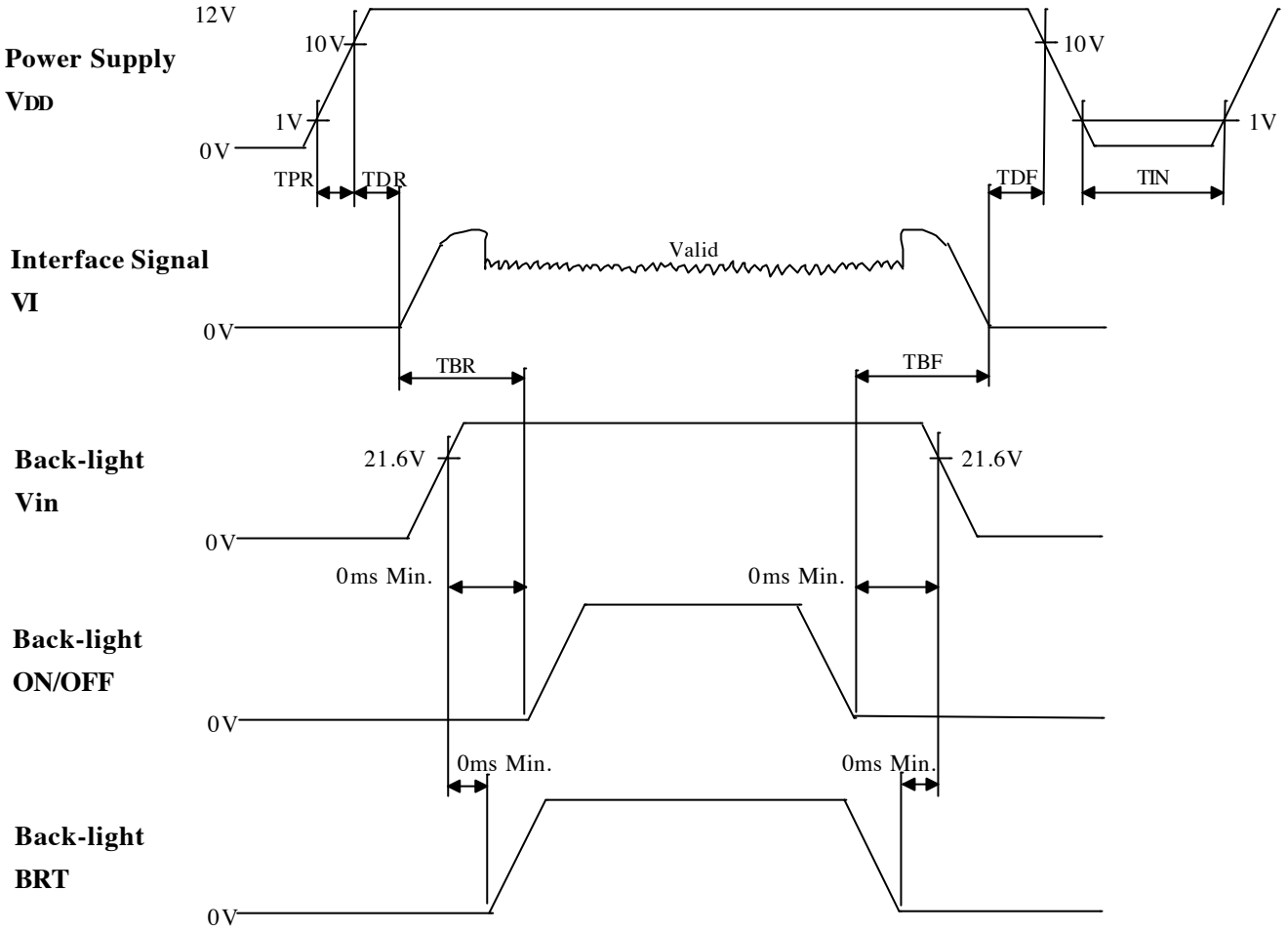
6.2 INTERFACE TIMING SPECIFICATIONS

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	fCLK	78	85	87	MHz	D=TCIL/TCIP
	Duty	D	0.35	0.5	0.65	-	
HSYNC	Frequency	fH	46.3	46.4	46.8	kHz	3)
	Period	THP	1410	1833	1992	TCIP	
	Width-Active	TWH	8	-	240	TCIP	
VSYNC	Frequency	fV	58	60	62	Hz	to HSYNC
	Set up Time	TSV	0	-	-	TCIP	
	Hold Time	THV	8	-	-	TCIP	
	Period	TVP	772	773	780	THP	
	Width-Active	TWV	1	-	120	THP	
DTMG	Horizontal Back porch	THBP	16	-	-	TCIP	1)
	Horizontal Front Porch	THFP	0	-	-	TCIP	
	Vertical Back Porch	TVBP	2	-	-	THP	
	Vertical Front porch	TVFP	2	-	-	THP	
	Width-Active	TWD	1366	1366	1366	TCIP	
COMMON	Set up Time	TSTC	5	-	-	ns	2)
	Hold Time	THTC	3	-	-	ns	

In addition to the above, these timing should conforms to the followings.

1) TVBP+TVFP≧4 THP
2) TSTC and THTC conforms to the specifications of LVDS transmitter.
   It is preferable to check the specifications of LVDS transmitter in your system.
3) Frequency of power supply for a CFL may cause the interference with HSYNC frequency and cause beat or flicker on the display.
   Therefore, HSYNC frequency shall be as different as possible from lamp frequency in order to avoid the interference.

6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Note

1)Timing of power supply voltage and input signals should be used under the following specifications.

0ms ≦ TPR ≦ 10ms

10ms ≦ TDR ≦ 50ms

0ms ≦ TDF ≦ 50ms

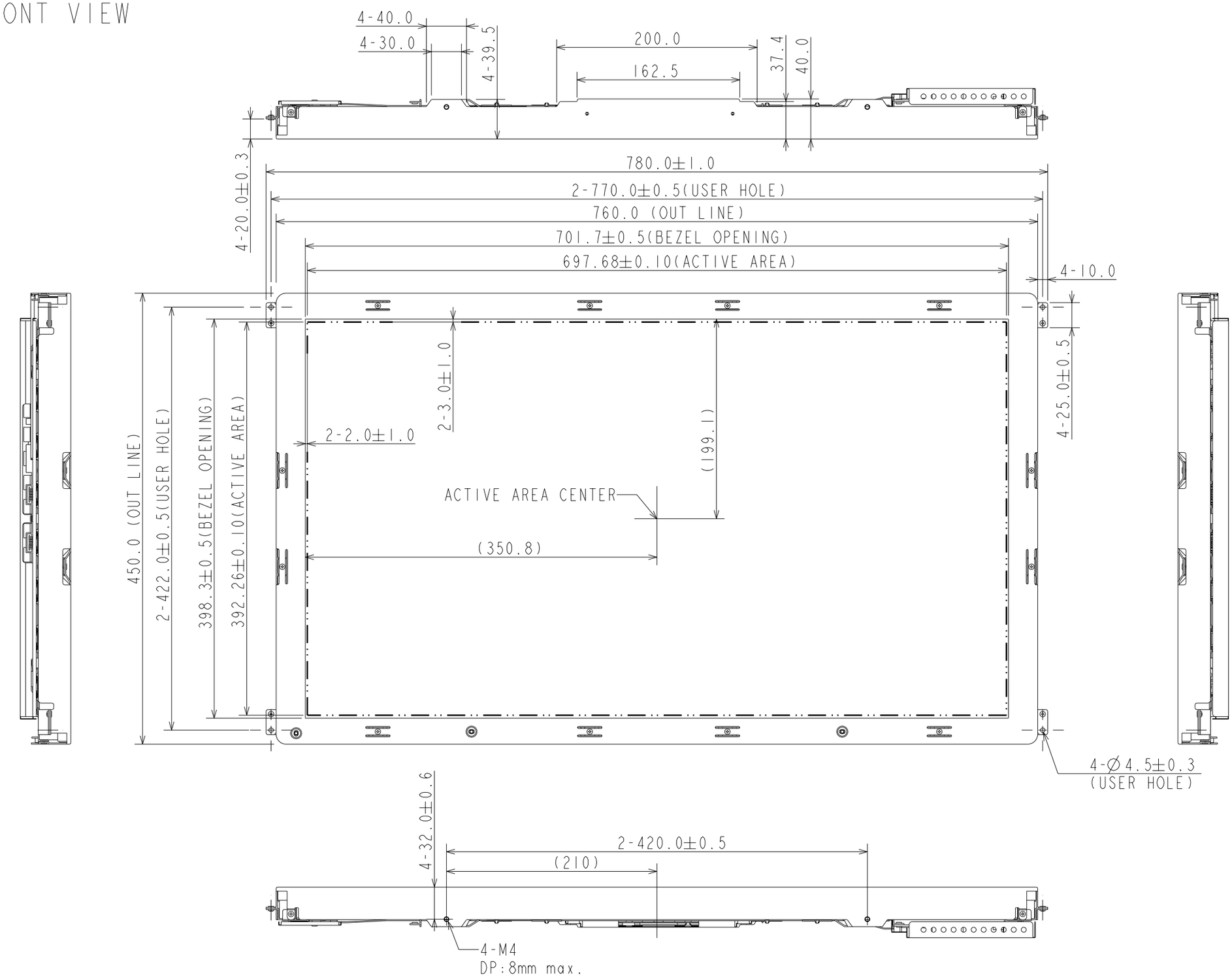
TIN ≧ 1s

200ms ≦ TBR

TBF ≦ 100ms

7. DIMENSIONAL OUTLINE

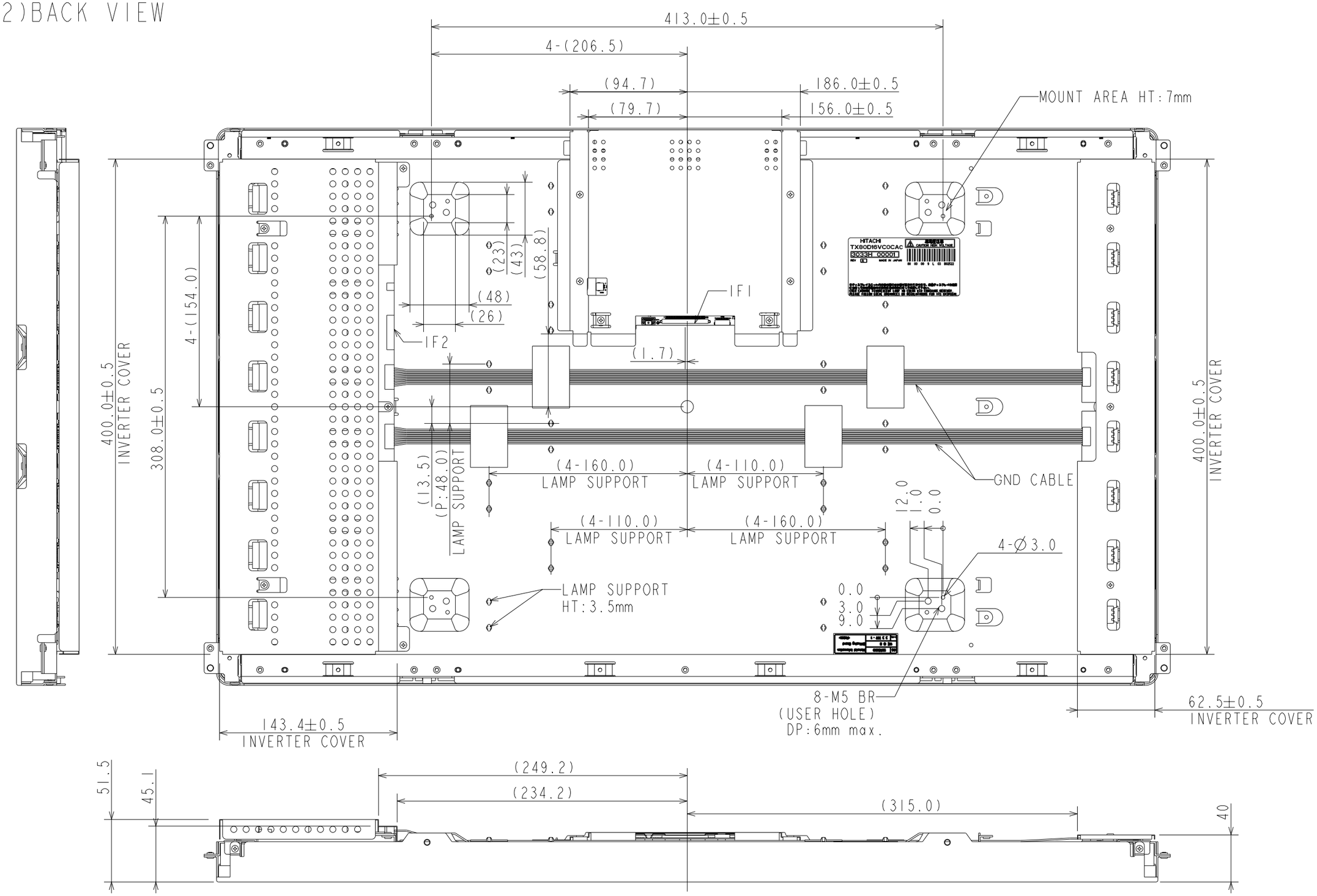
(1) FRONT VIEW



Note 1)The dimension in a parenthesis is a reference value.
2)Unspecified tolerance to be ±0.8

Hitachi Displays, Ltd.	Date	Oct 13,2004	Sh. No.	3284STD - 2342 - 1	Page	10-1/2

(2)BACK VIEW

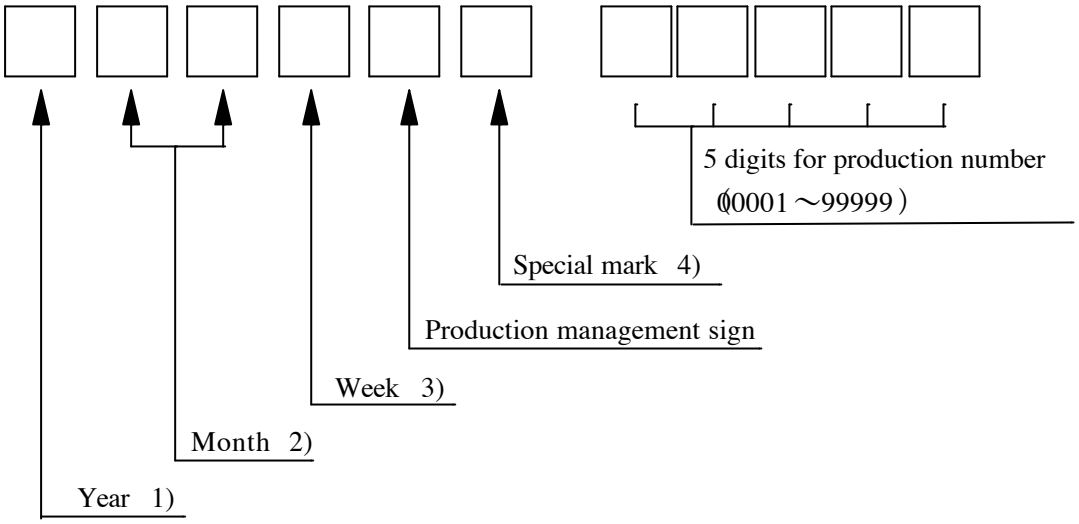


Note 1)The dimension in a parenthesis is a reference value.
2)Unspecified tolerance to be ±0.8

Hitachi Displays, Ltd.	Date	Oct 13,2004	Sh. No.	3284STD - 2342 - 1	Page	10-2/2

8. DESIGNATION OF LOT MARK

8.1 LOT MARK



Notes

1)

Year	Mark
2004	4
2005	5
2006	6
2007	7

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week (Day)	Mark
1～7	1
8～14	2
15～21	3
22～28	4
29～31	5

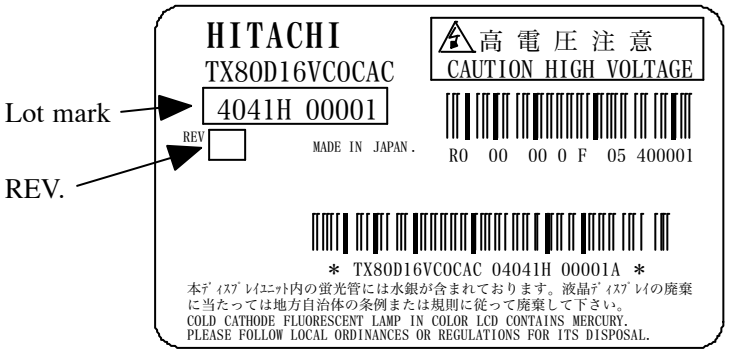
4) It is the mark that was opened up by production person to take correspondence with production number.

8.2 Revision (REV.) control

REV. is the column for manufacturing convenience. A-Z except I and O may be written on this column.

8.3 Location of lot mark

Lot mark is printed on a label. The label is on the metallic bezel as shown in 7. External Dimensional. The style of character will be changed without notice.



10. PRECAUTION

Please pay attention to the followings when a Super-TFT module with a back-light unit is used, handled and mounted.

10.1 Precaution to handling and mounting

(1) Applying strong force to a part of the module may cause partial deformation of frame or mold, and cause damage to the display.

(2) The module should gently and firmly be held by both hands. Never hold by just one hand in order to avoid any internal damage. Never drop or hit the module.

(3) The module should be installed with mounting holes at each corner of a module.

(4) Uneven force such as twisted stress should not be applied to a module when a module is mounted on the cover case. The cover case must have sufficient strength so that external force can not be transmitted directly to a module.

(5) It is recommended to leave a space between a module and a holding board of a module so that partial force is not applied to a module.

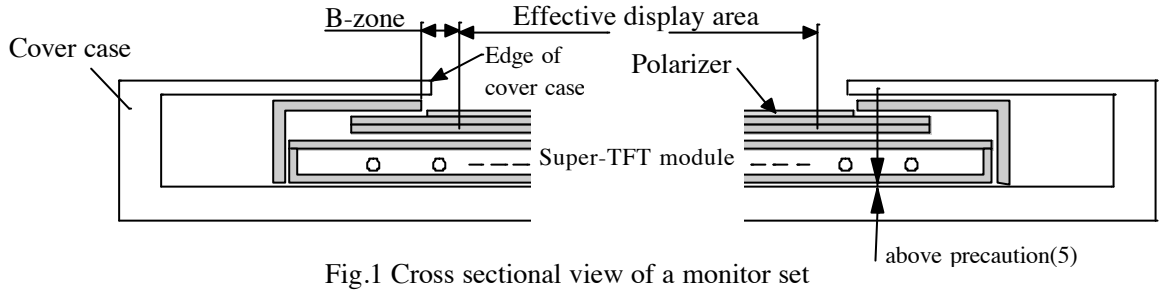


Fig.1 Cross sectional view of a monitor set

(6) The edge of a cover case should be located inside more than 1mm from the edge of a module front frame.

(7) A transparent protective plate should be added on the display area of a module in order to protect a polarizer and Super-TFT cell. The transparent protective plate should have sufficient strength so that the plate can not touch a module by external force.

(8) Materials included acetic acid and choline should not be used for a cover case as well as other parts and boards near a module. Acetic acid attacks a polarizer. Choline attacks electric circuits due to electro-chemical reaction.

(9) The polarizer on a TFT cell should carefully be handled due to its softness, and should not be touched, pushed or rubbed with glass, tweezers or anything harder than HB pencil lead. The surface of a polarizer should not be touched and rubbed with bare hand, greasy clothes or dusty clothes.

(10) The surface of a polarizer should be gently wiped with absorbent cotton, chamois or other soft materials slightly contained petroleum benzene when the surface becomes dirty. Normal-hexane as cleaning chemicals is recommended in order to clean adhesives which fix front/rear polarizers on a Super-TFT cell. Other cleaning chemicals such as acetone, toluen and alcohol should not be used to clean adhesives because they cause chemical damage to a polarizer.

(11) Saliva or water drops should be immediately wiped off. Otherwise, the portion of a polarizer may be deformed and its color may be faded.

(12) The module should not be opened or modified. It may cause not to operate properly.

(13) Metallic bezel of a module should not be handled with bare hand or dirty gloves. Otherwise, color of a metallic frame may become dirty during its storage. It is recommended to use clean soft gloves and clean finger stalls when a module is handled at incoming inspection process and production (assembly) process.
(14) Lamp(CCFL) cables should not be pulled and held.

10.2 Precaution to operation

(1) The ambient temperature near the operated module should be satisfied with the absolute maximum ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.
(2) The spike noise causes the mis-operation of a module. The level of spike noise should be as follows:
-200mV<=over- and under- shoot of VDD<= +200mV
VDD including over- and under- shoot should be satisfied with the absolute maximum ratings.
(3) Optical response time, luminance and chromaticity depend on the temperature of a Super-TFT module. Response time and saturation time of CCFL luminance become longer at lower temperature operation.
(4) Sudden temperature change may cause dew on and/or in the a module. Dew males damage to a polarizer and/or electrical contacting portion. Dew causes fading of displayed quality.
(5) Fixed patterns displayed on a module for a long time may cause after-image. It will be recovered soon.
(6) A module has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be effective to minimize the interference.
(7) Noise may be heard when a back-light is operated. If necessary, sufficient suppression should be done by system manufacturers.
(8) The module should not be connected or removed while a main system works.
(9) Inserting or pulling I/F connectors causes any trouble when power supply and signal dates are on-state.I/F connectors should be inserted and pulled after power supply and signal dates are turned off.

10.3 Electrostatic discharge control

(1) Since a module consists of a Super-TFT cell and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling a module should be grounded through adequate methods such as a list band. I/F connector pins should not be touched directly with bare hands.
(2) Protection film for a polarizer on a module should be slowly peeled off so that the electrostatic charge can be minimized.

10.4 Precaution to strong light exposure

(1) A module should not be exposed under strong light. Otherwise, characteristics of a polarizer and color filter in a module may be degraded.

10.5 Precaution to storage

When modules for replacement are stored for a long time, following precautions should be taken care of:
(1) Modules should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage. Modules should be stored at 0 to 35°C at normal humidity (60%RH or less).
(2) The surface of polarizers should not come in contact with any other object. It is recommended that modules should be stored in the Hitachi's shipping box.

10.6 Precaution to handling protection film

(1) The protection film for polarizers should be pealed off slowly and carefully by persons who are electrically grounded with adequate methods such as a list band. Besides, ionized air should be blown over during peeling action. Dusts on a polarizer should be blown off by an ionized nitrogen gun and so on.

(2) The protection film should be peeling off without rubbing it to the polarizer. Because, if the film is rubbed together with the polarizer, since the film is attached to the polarizer with a small amount of adhesive, the adhesive may remain on a polarizer.

(3) The module with protection film should be stored on the conditions explained in 10.5 (1). However , in case that the storage time is too long, adhesive may remain on a polarizer even after a protection film is peeled off. Besides, in case that a module is stored at higher temperature and/or higher humidity, adhesive may remain on a polarizer. The remained adhesive may cause non-uniformity of display image.

(4) The adhesive can be removed easily with Normal-Hexane. The remained adhesive or its vestige on the polarizer should be wiped off with absorbent cotton or other soft materials such as chamois slightly contained Normal-Hexane.

10.7 Safety

(1) Since a Super-TFT cell and lamps are made of glass, handling to the broken module should be taken care sufficiently in order not to be injured. Hands touched liquid crystal from a broken cell should be washed sufficiently.

(2) The module should not be taken apart during operation so that back-light drives by high voltage.

10.8 Environmental protection

(1) The Super-TFT module contains cold cathode fluorescent lamps. Please follow local ordinance or regulations for its disposal.

(2) Flexible circuits board and printed circuits board used in a module contain small amount of lead. Please follow local ordinance or regulations for its disposal.

10.9 Use restrictions and limitations

(1) This product is not authorized for use in life support devices or systems, military applications or other applications which pose a significant risk of personal injury.

(2) In no event shall Hitachi, Ltd., be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility thereof in advance. These limitations apply to all causes of action in the aggregate, including without limitation breach of contact, breach of warranty, negligence, strict liability, misrepresentation and other torts.

10.10 Others

(1) Electrical components which may not affect electrical performance are subjective to change without notice because of their availability.